Welcome To

ISSCC 2014
Session 14
Millimeter-Wave and Terahertz Techniques

A 0.9V 20.9dBm 22.3%-PAE E-band Power Amplifier with Broadband Parallel-Series Power Combiner in 40nm CMOS

Dixian Zhao, Patrick Reynaert

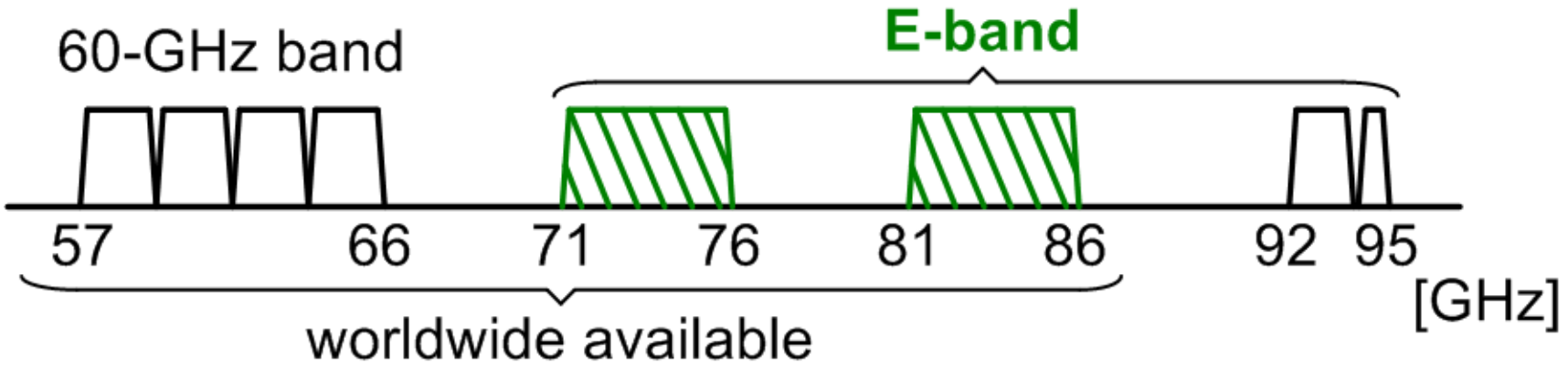
KU Leuven, ESAT-MICAS, Belgium

Outline

- Introduction
- PA Design and Implementation
- Measurement Results
- Conclusion

E-band Technology

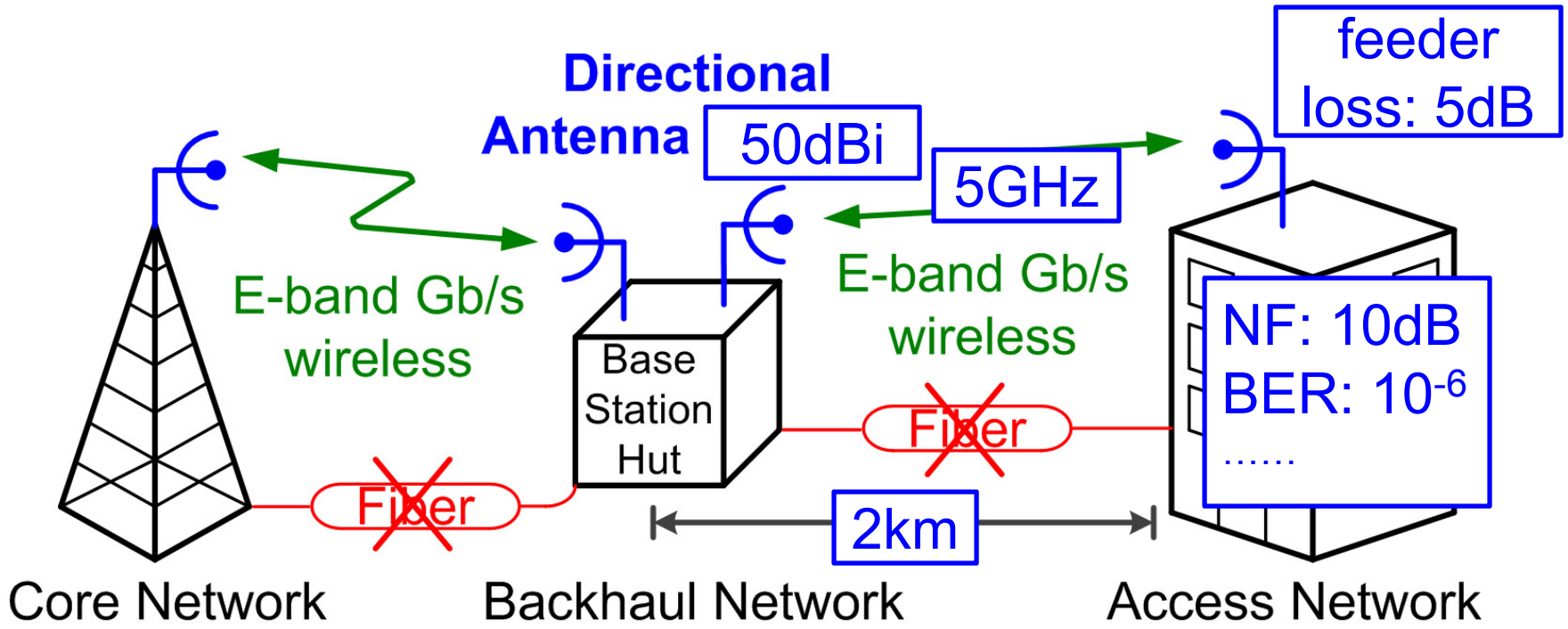
- **Allocation: 71-76 & 81-86 GHz (2×5GHz BW).**
- **Licensed band: regulatory protection.**
- **Propagation characteristics**
  - low atmospheric attenuation (0.2dB/km)
  - rain attenuation (10dB/km for heavy rain)
  - unaffected by other deteriorations (e.g., fog, dust…)



E-band Applications

- **Mobile backhaul**
- **Enterprise connections**
- **Fiber extension / replacement**

→ low cost, easy to install, fast paybacks…



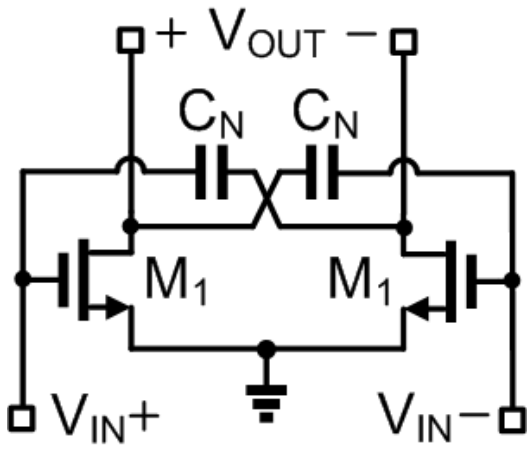
E-band PA Requirements

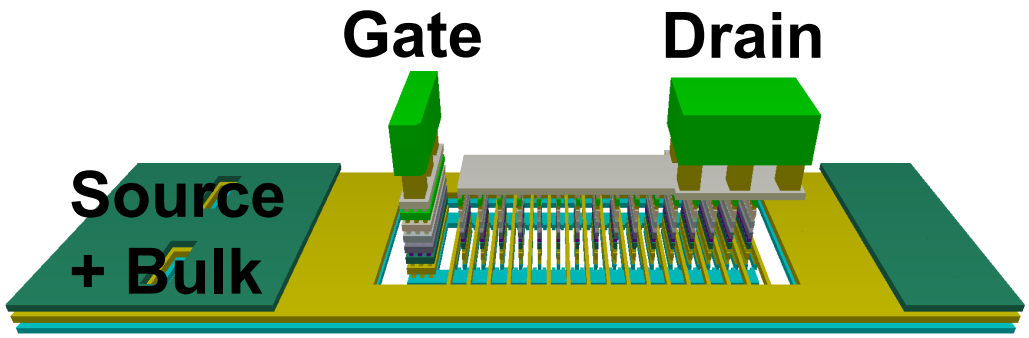
- **Output power = 20dBm (2km)**
  - 64QAM: max. data rate 30Gb/s.
  - QPSK: max. data rate 10Gb/s (heavy rain).
- **Large signal -1dB BW = 15GHz**
  - constant P_{OUT} across 71-76 & 81-86 GHz.
  - FDD: 10-GHz spacing between TX/RX.
- **Small signal -3dB BW = 15GHz**
  - broadband communication in each sub-band.
- **High efficiency**

Outline

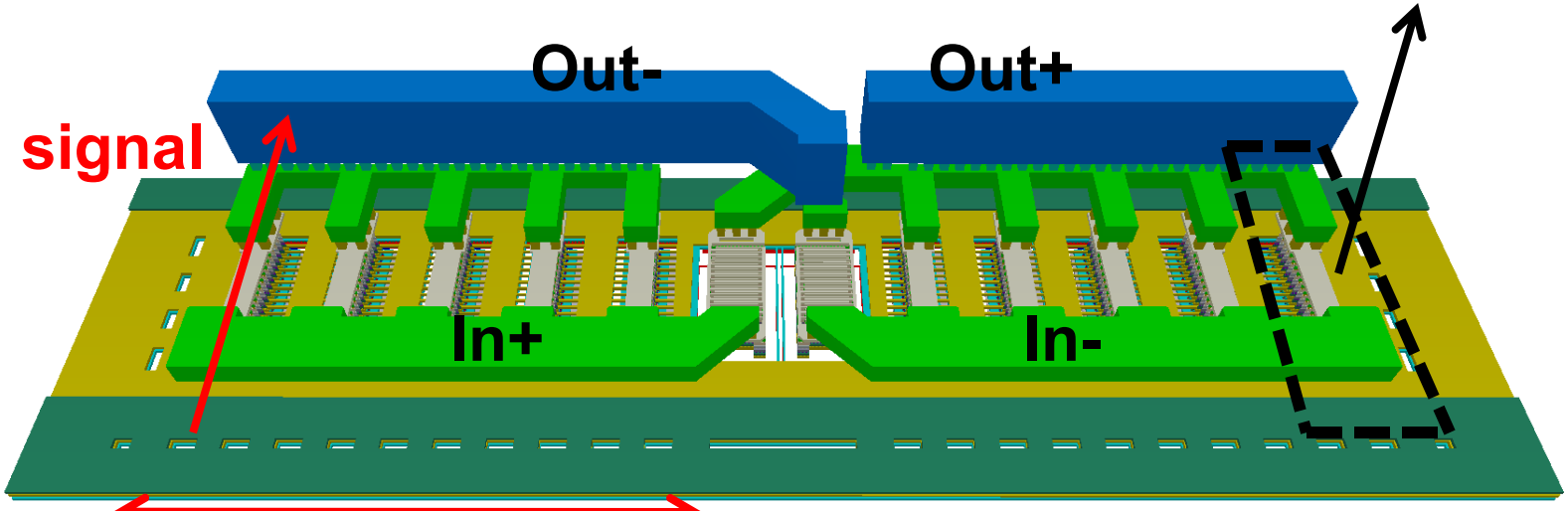
- Introduction
- **PA Design and Implementation**
- Measurement Results
- Comparison and Conclusion

Neutralized Amplifier Layout



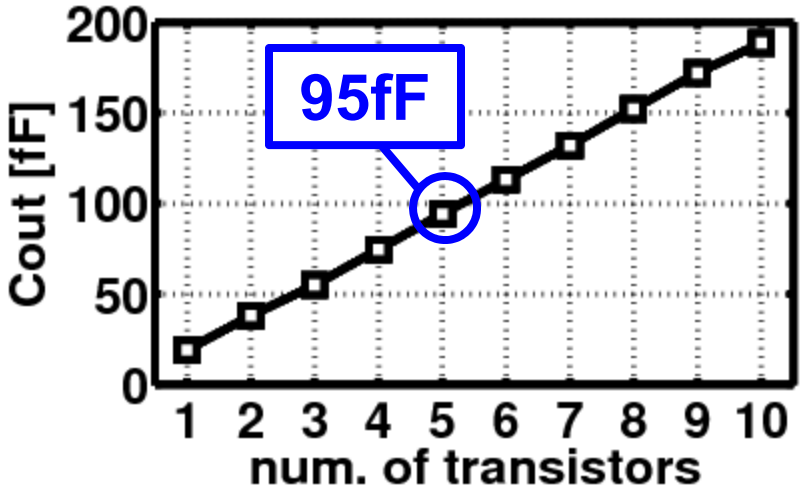


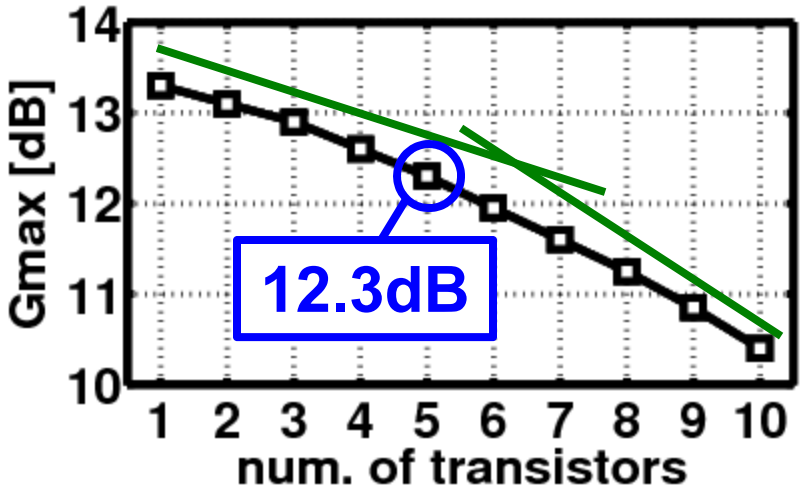
[Zhao, JSSC13]

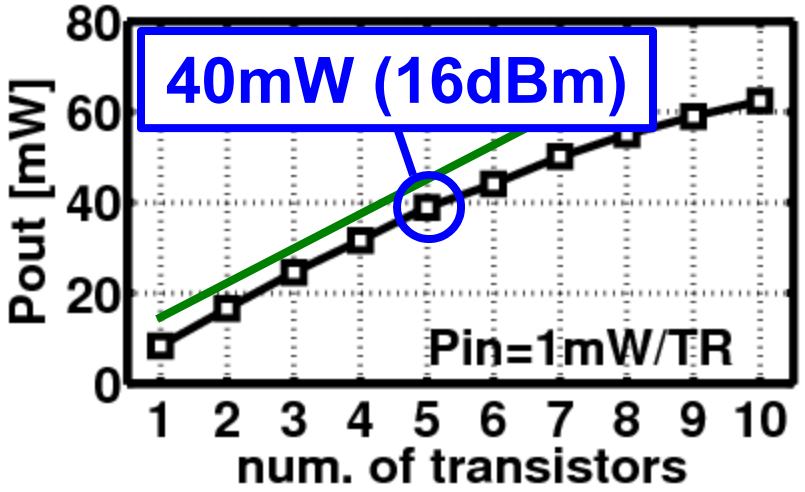


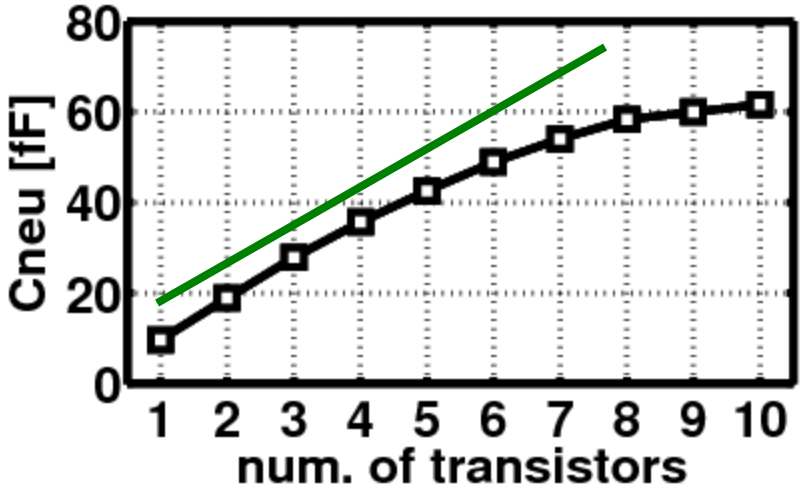
176μm/40nm (5×35.2μm)

Metrics vs. number of unit transistors

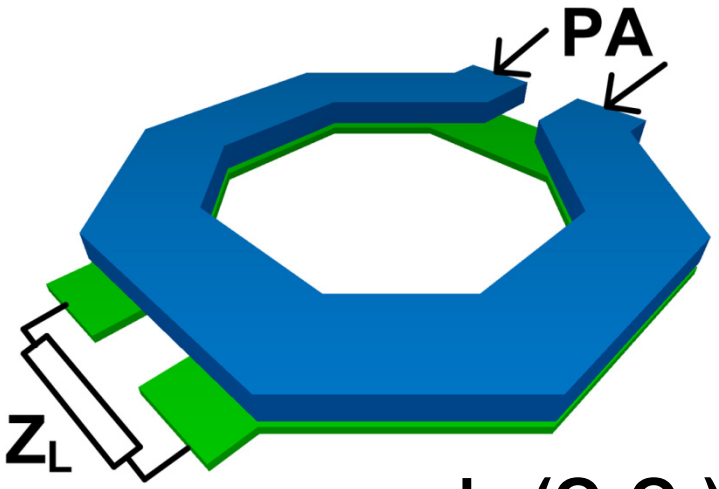




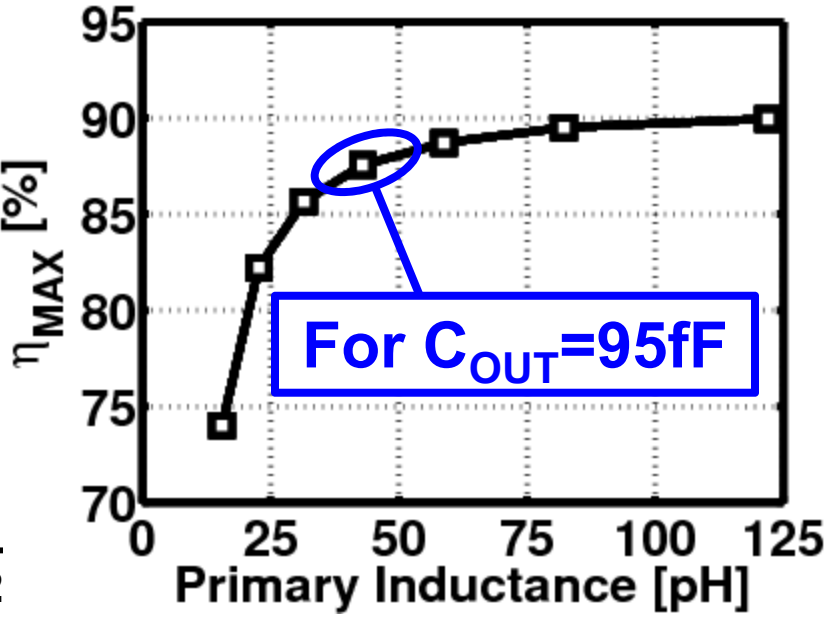




Transformer Efficiency

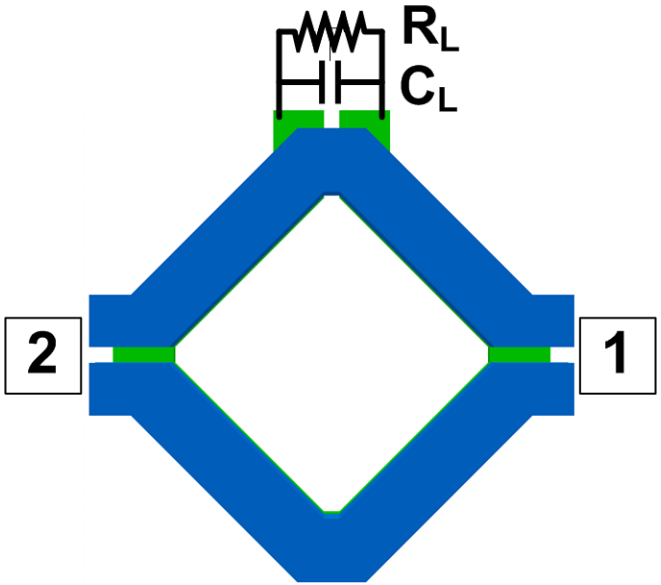


$$\eta_{MAX} \approx \frac{k_m(Q_pQ_s)^{1/2}}{2+k_m(Q_pQ_s)^{1/2}}$$

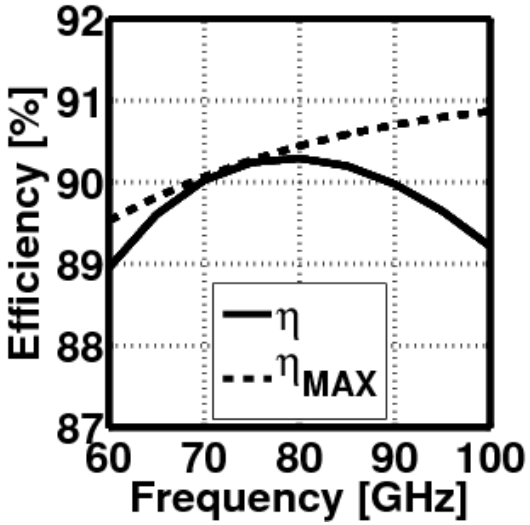


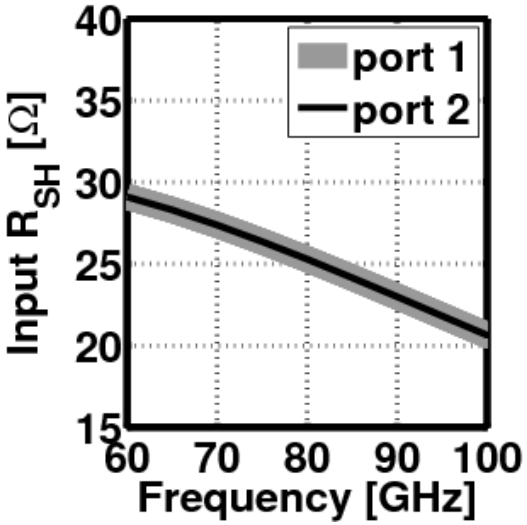
- Large transistor size → small transformer → low η.
- Transistor size: 176μm/40nm (5×35.2μm) → 16dBm.
- 4-way power combiner for more than 20dBm P_{OUT}.

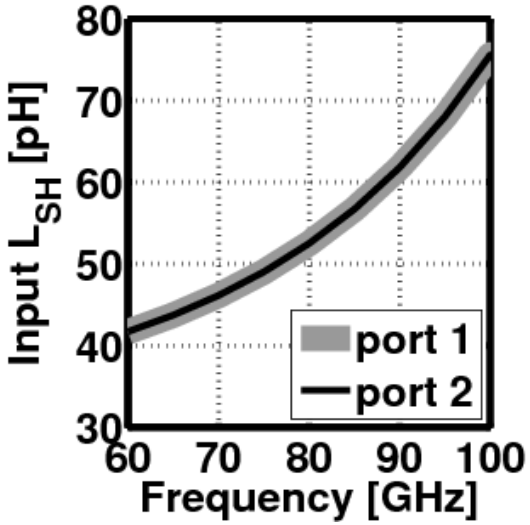
2-Way Series Combiner



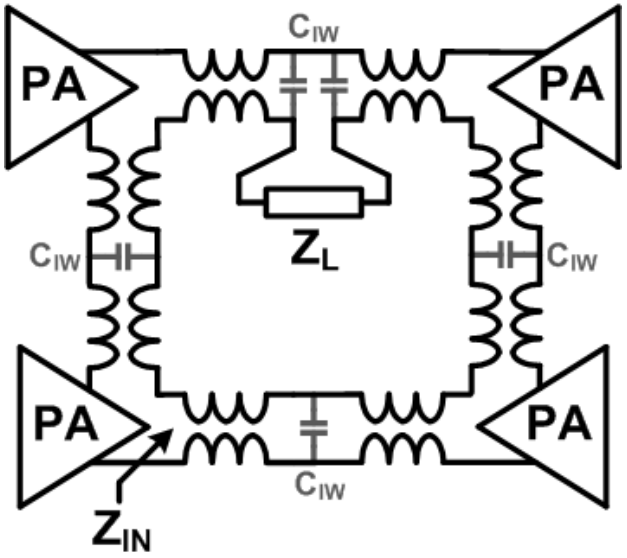
- **DAT-based [Aoki, 2002]**
  - compact & high η
- **Broadband matching**



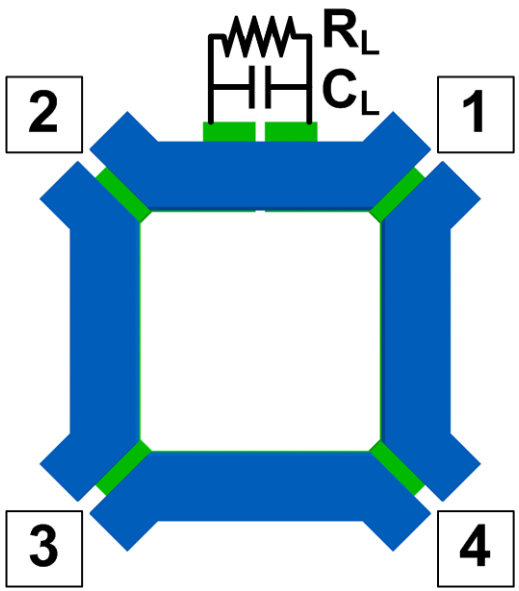




N-Way Series Combiner Challenges

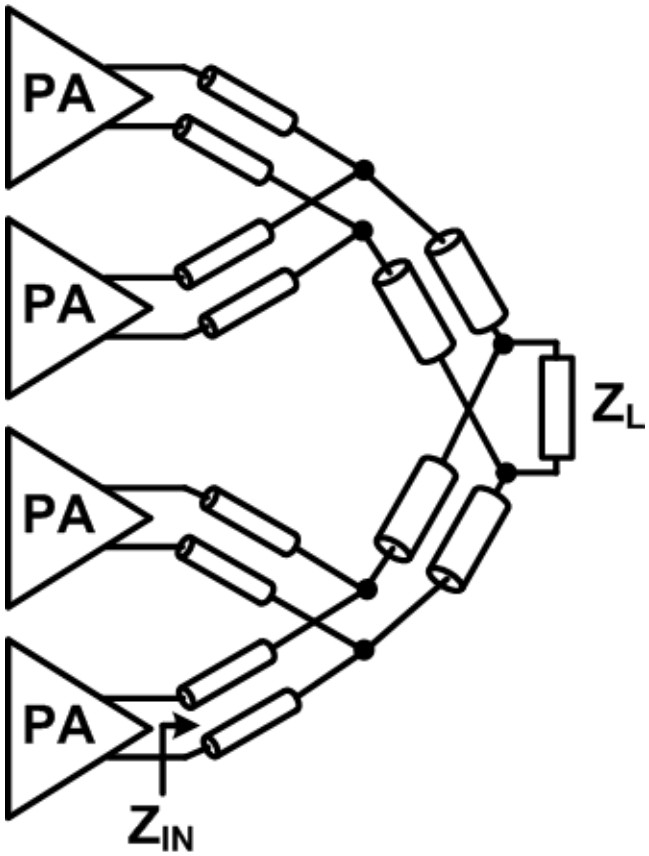


1. **$Z_{IN} \approx 1/N \times Z_L$**
   N = 4: Z_{IN} = 12.5Ω
   → large transistor
   → low gain & η



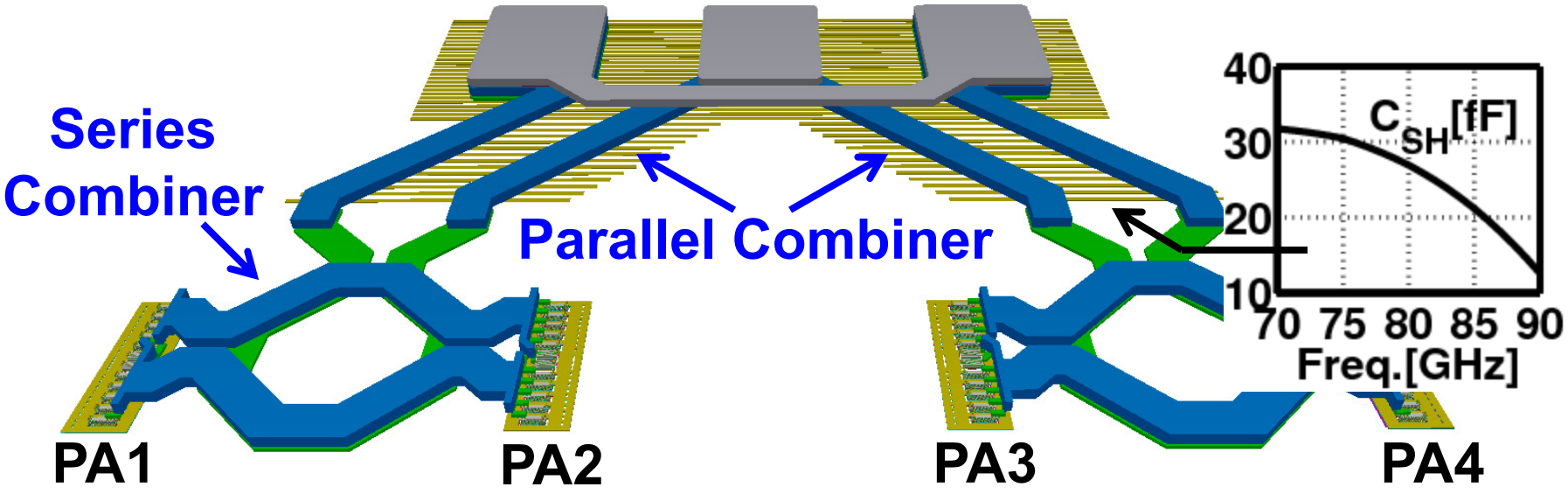
2. **Interwinding C_{IW} → unbalanced Z_{IN}**
   port 1, 2: R_{SH} = 22Ω , L_{SH} = 22pH
   port 3, 4: R_{SH} = 9Ω, L_{SH} = 26pH
3. **Complex input signal distribution**

N-Way Parallel Combiner



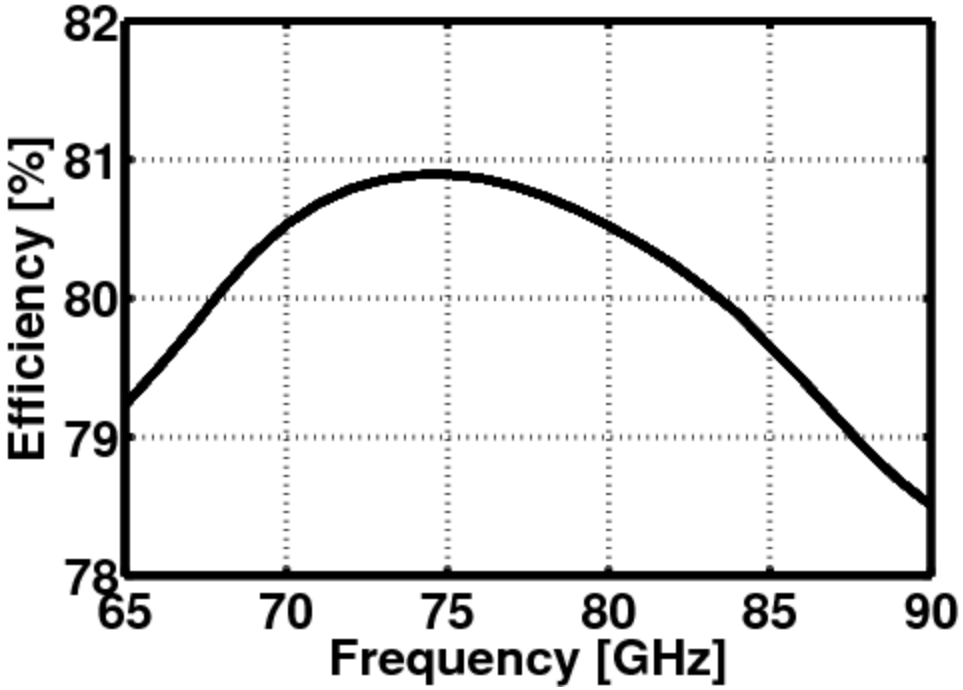
- **T-line-based**
- ✓ **Signal distribution**
- ✓ **Balanced Z_{IN}**
- × **$Z_{IN} \approx N \times Z_L$**
  N = 4: Z_{IN} = 200Ω
  → small transistor
  → low P_{OUT}
- × **↑N:** ↑loss, ↑area & ↓BW

Proposed Parallel-Series Combiner



series	parallel	parallel-series
small footprint	easy distribution	compact floor plan
Z_{IN} ↓	Z_{IN} ↑	opt. transistor size
high η & P_{OUT}	balanced Z_{IN}	efficiently adds 4 PAs

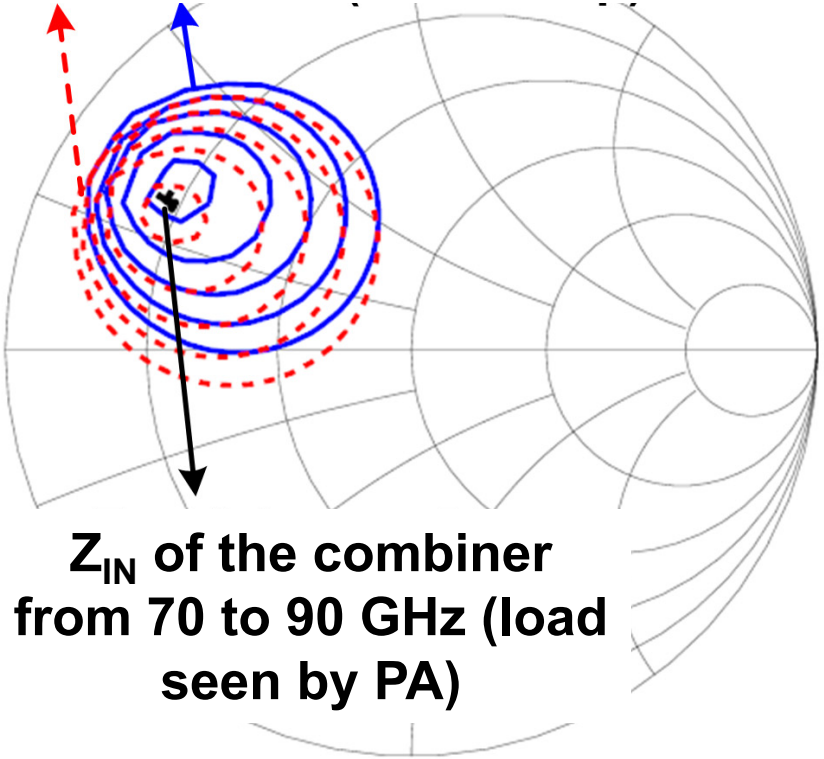
Combiner Efficiency (η)



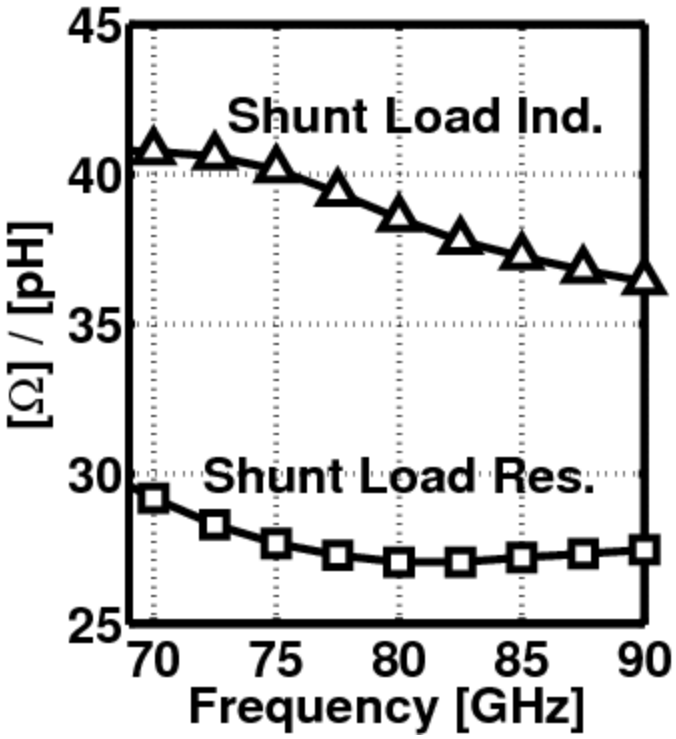
- **Parallel-series combiner + RF pads.**
- **Insertion loss < 1dB from 66 GHz to 86GHz.**

Broadband Matching

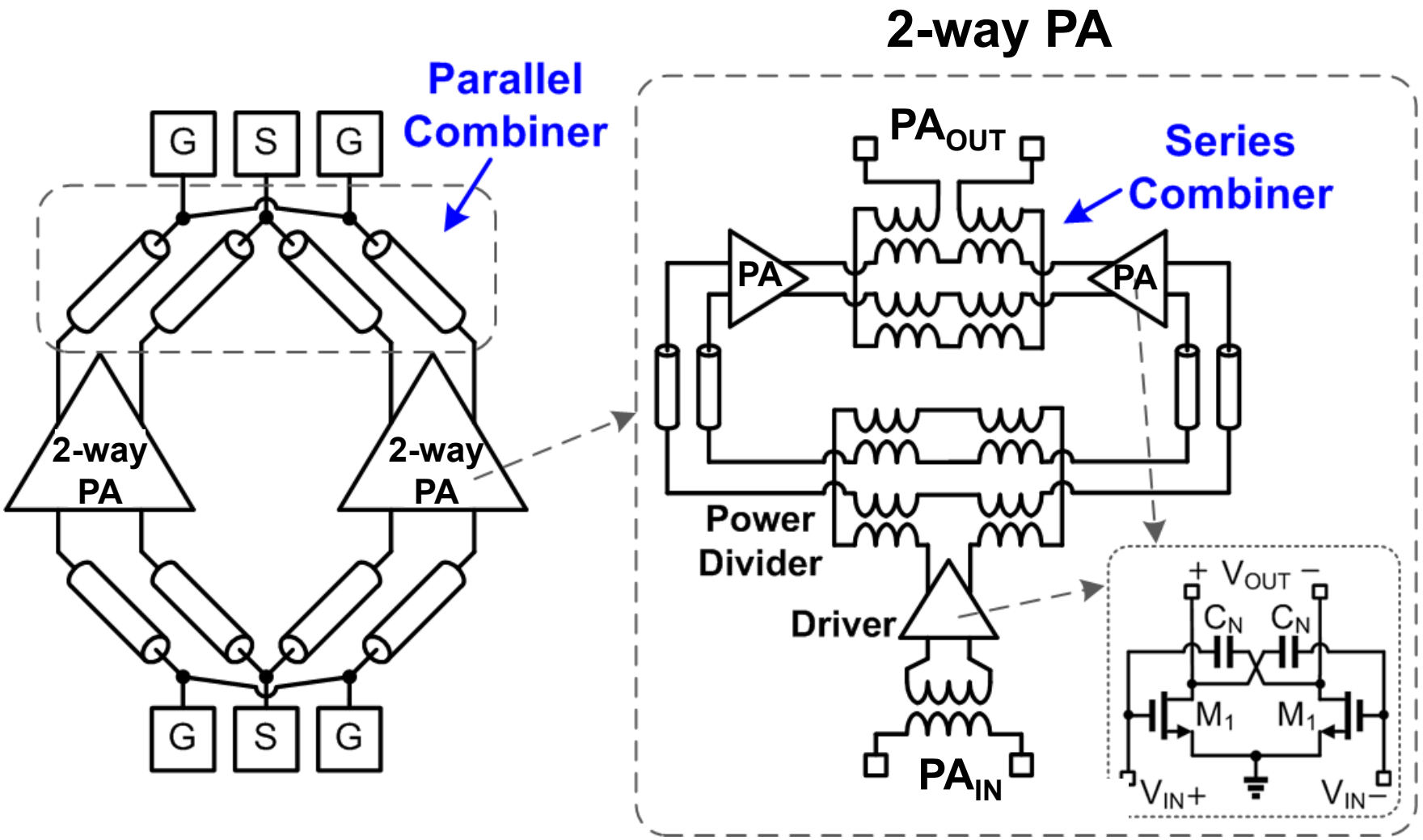
P_{OUT} contours of the PA at 83 & 74 GHz (0.5dB/step)



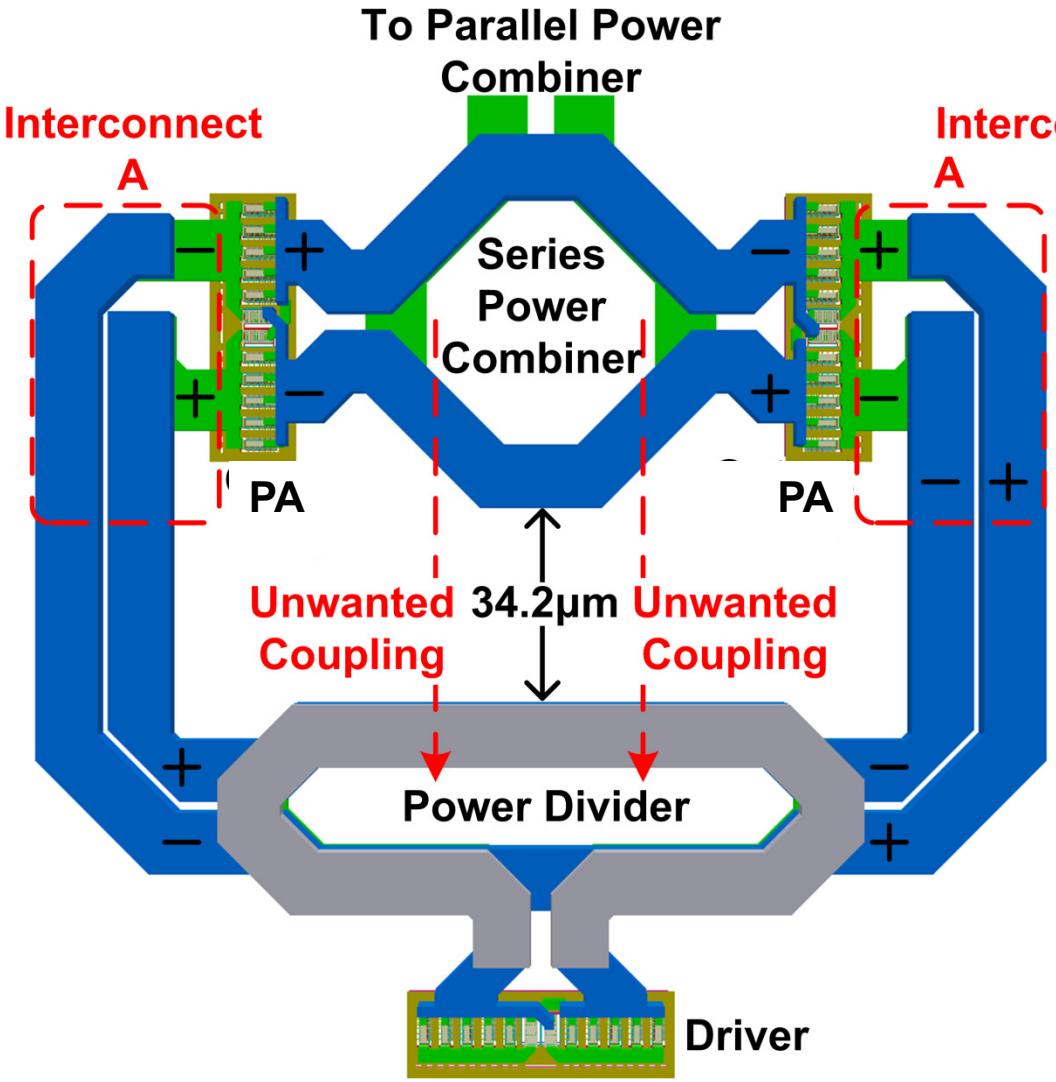
Z_{IN} of the combiner from 70 to 90 GHz (load seen by PA)

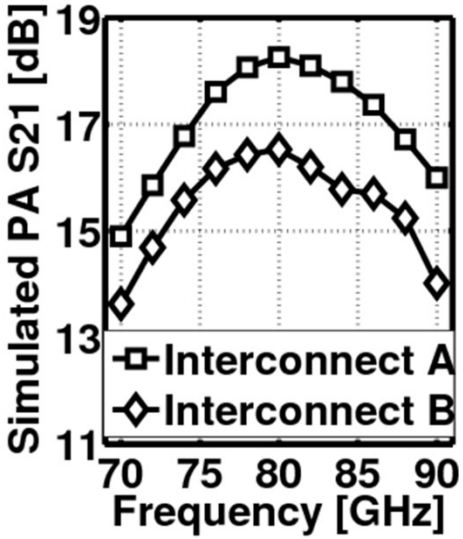


Complete PA Circuit



Mutual Coupling





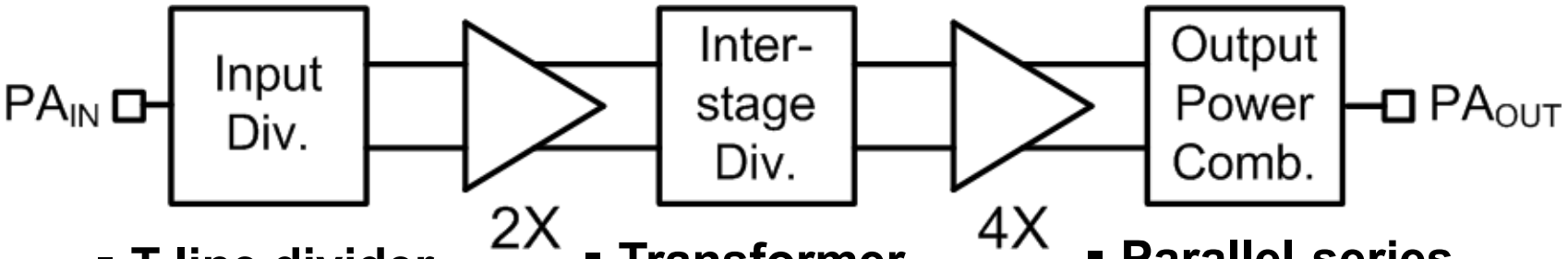
Compact floor plan:

↓ passive loss

↓ chip area

↑ mutual coupling

Broadband E-band PA Design

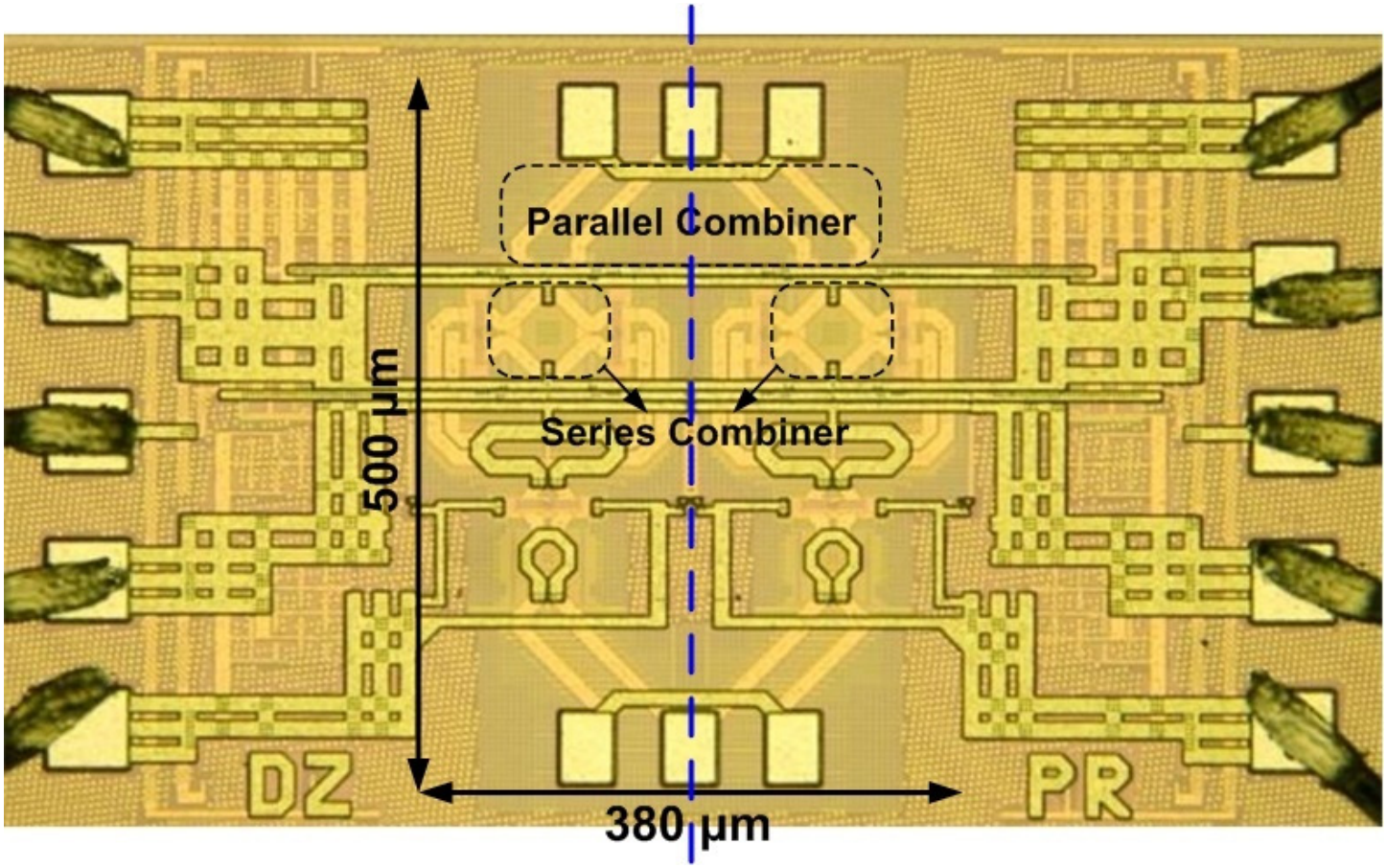


- **Transistor layout and amplifier optimization.**
- **Output: parallel-series power combiner.**
- **Inter-stage: sufficient linear drive power.**
- **Input: T-line based power divider ($\downarrow Z_{IN}$).**

Outline

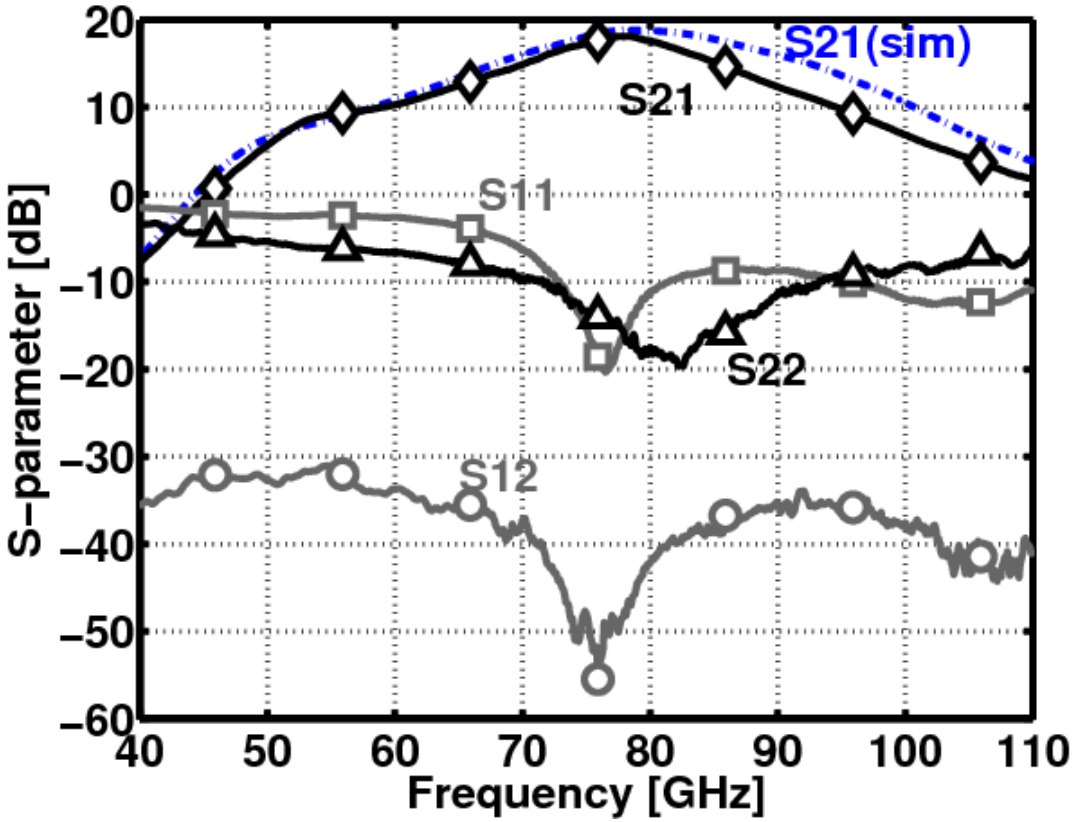
- Introduction
- PA Design and Implementation
- **Measurement Results**
- Comparison and Conclusion

Chip Micrograph



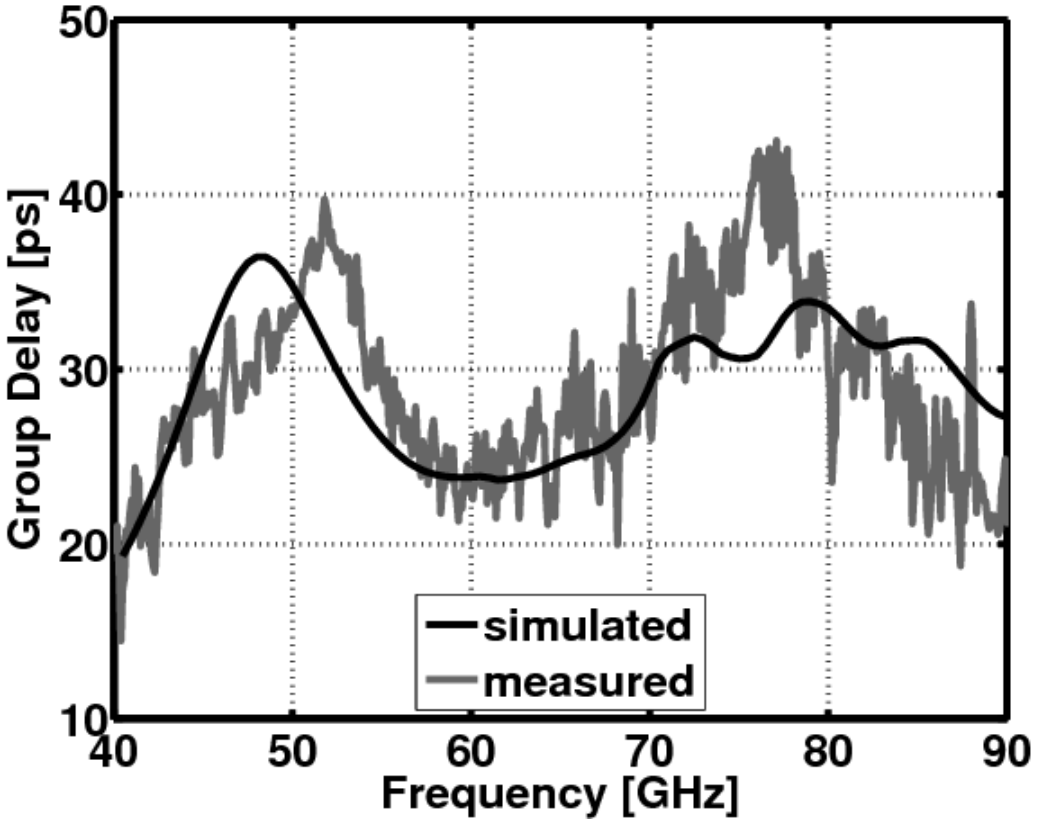
- 40nm CMOS GP.
- Area: 0.19 mm^2 (incl. RF pads).
- Two 2-way PAs symmetrical against the central line.

Measured S-parameters



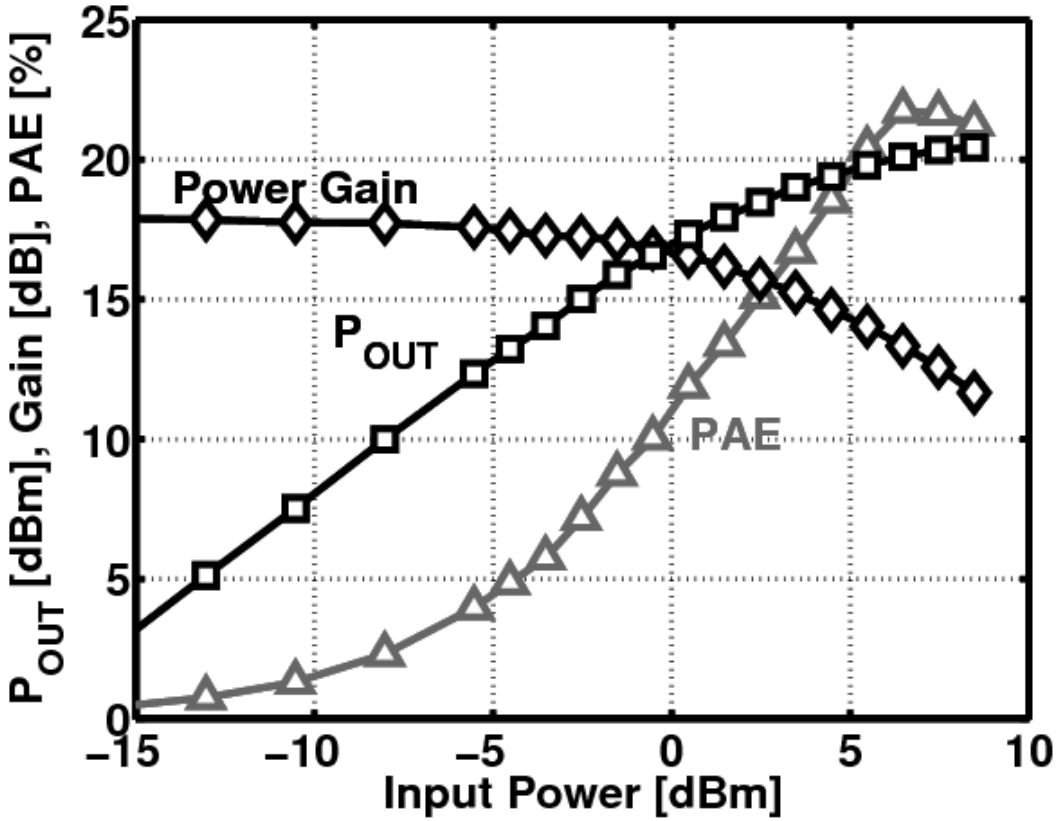
- S_{11}, S_{22}, S_{12} < -8, -10, -37 dB from 71 to 86 GHz.
- Unconditional stable from 0.1-110 GHz (μ > 1).

Measured Group Delay



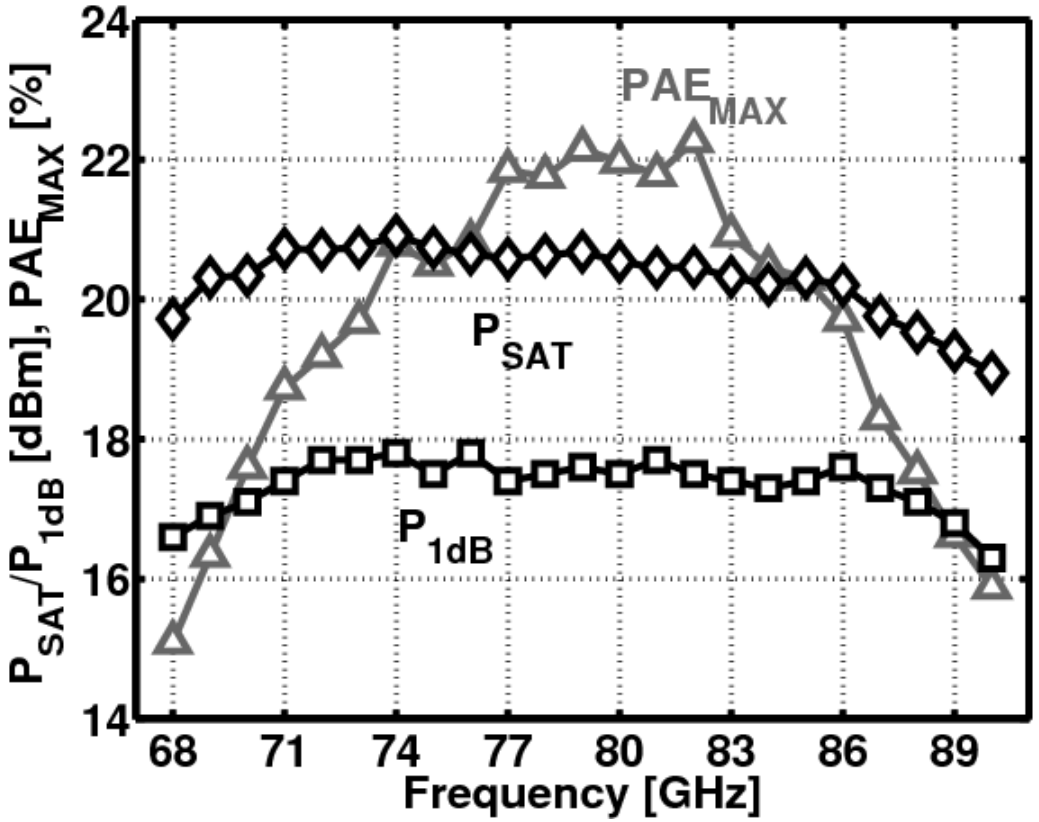
- Delay variation of 22.6ps from 71 to 86 GHz.
- Delay variation < 13ps in 71−76 & 81-86GHz bands.

Measured P_{OUT} & PAE



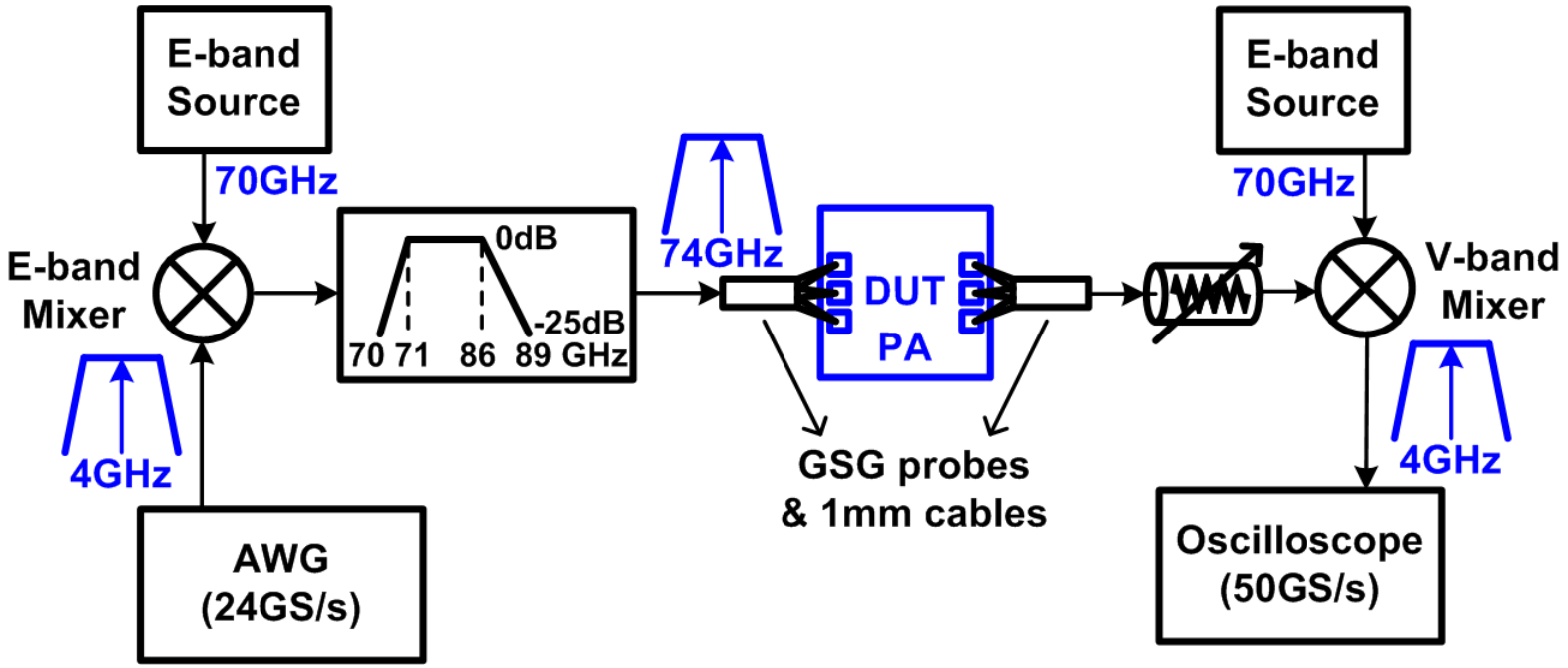
- dc power consumption: 375 mW @ 0.9 V supply.
- P_{1dB}=17.4dBm, P_{SAT}= 20.4dBm, PAE_{MAX}=22% @80GHz.

P_{SAT}, P_{1dB}, PAE vs. Frequency



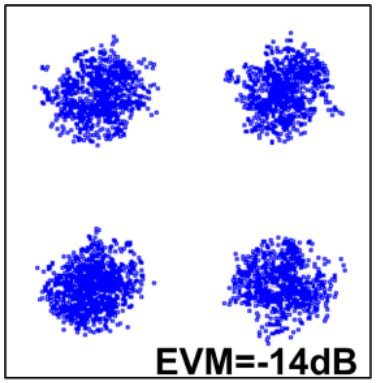
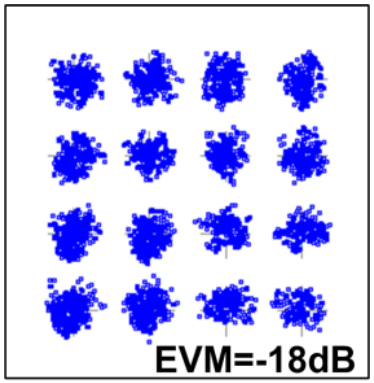
- P_{1dB} varies only 0.5 dB (71-87 GHz).
- Nearly uniform performance across E-band.

Modulated Signal Measurement



- **SSB up-converter = balanced Mixer + BPF.**
- **Measurement performed w/ & w/o DUT (PA).**

QPSK & 16QAM

Modulation	QPSK	16QAM
PAPR	3.9 dB	6.5 dB
Constellation [2048 points]		
Data Rate	5 Gb/s	2 Gb/s
EVM (w/ DUT)	-14 dB	-18 dB
EVM (w/o DUT)	-16 dB	-18.5 dB
Average P_{OUT}	13.0 dBm	12.5 dBm
dc Power	395 mW	390 mW

Comparison

	This Work	ISSCC12	TMTT13	ISSCC06	JSSC12	TMTT13
Technology	**40nm CMOS**	65nm CMOS	65nm CMOS	130nm SiGe	130nm SiGe	180nm SiGe
V_{DD} [V]	**0.9**	1.0	2	-2.5/0.8	2.5	4
Freq. [GHz]	**70.3-85.5**	79	77	85	84	83
Max. S_{21} [dB]	**18.1**	24.2	20.9	9	27	25
BW_{-3dB} [GHz]	**15.2**	10	N/A	>18‡	8	9.6
P_{SAT} [dBm]	**20.9**	19.3 #	15.8	21	18	14.7
PAE_{MAX} [%]	**22.3**	19.2 #	15.2	4 (η_{Drain})	9	8.1
P_{1dB} [dBm]	**17.8**	16.4 #	13	N/A	16	12.5
P_{1dB} variation [dB (GHz)]	**0.5 (71-87)**	N/A	2 (75-82)	N/A	2 (75-90)	1 (75-88)
Area [mm^2]	**0.19**	0.855	0.21	2.4†	0.68†	0.34
Path combined	**4-way diff.**	8-way	2-way diff.	4-way	2-way diff.	2-way
Topology	**2-stage CS**	4-s. CS	2-s. CASC	DA /CASC	3-s. CB	2-s. CA

The loss of the on-chip output balun was de-embedded from the measured P_{SAT}, P_{1dB} and PAE_{MAX}.
‡ The gain is only shown from 72 to 90 GHz. † Include the area of DC pads.

Conclusion

- **E-band for long-haul high-speed PTP**
- **mm-Wave PA customized for E-band**
  - optimized transistor layout & transistor size
  - broadband parallel-series combiner
  - compact floor plan
- **Highlights → uniform performance in E-band**
  - 18dB gain with 15 GHz BW_{-3dB}
  - P_{SAT} > 20 dBm (68.5-86.5 GHz)
  - P_{1dB} = 17.55±0.25 dBm (71-86 GHz)
  - PAE_{MAX}= 20.5±1.8% (71-86 GHz).

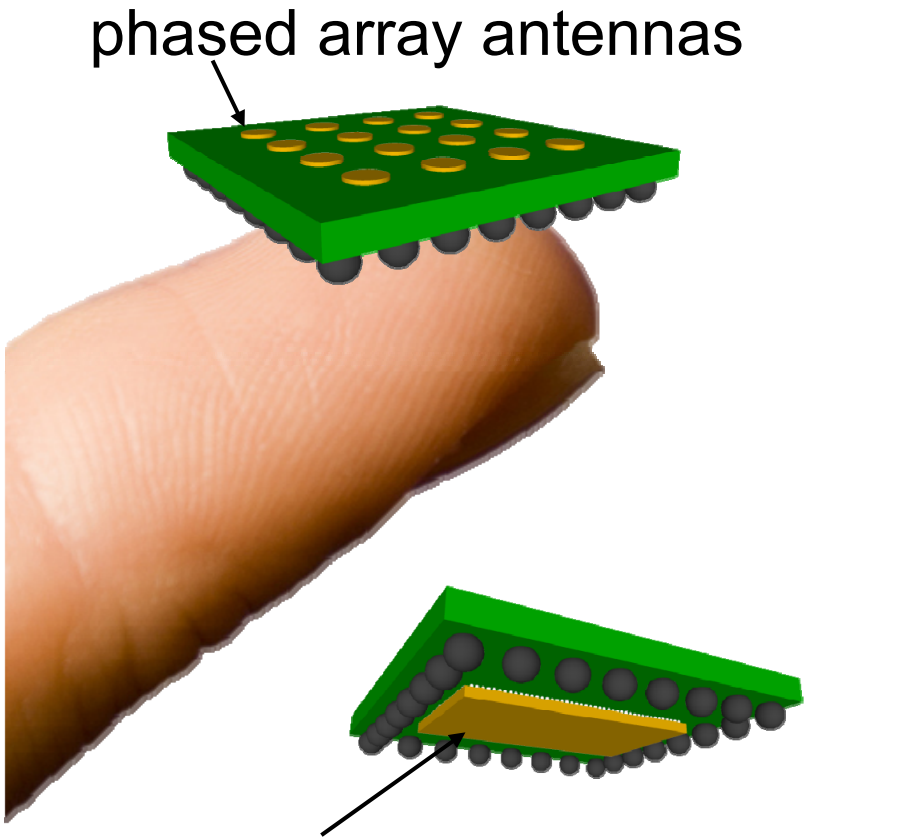
A 79GHz Phase-Modulated 4GHz-BW CW Radar TX in 28nm CMOS

V. Giannini[1], D. Guermandi[1], Q. Shi[1,2], K. Vaesen[1],
B. Parvais[1], W. Van Thillo[1], A. Bourdoux[1],
C. Soens[1], J. Craninckx[1], P. Wambacq[1,2]

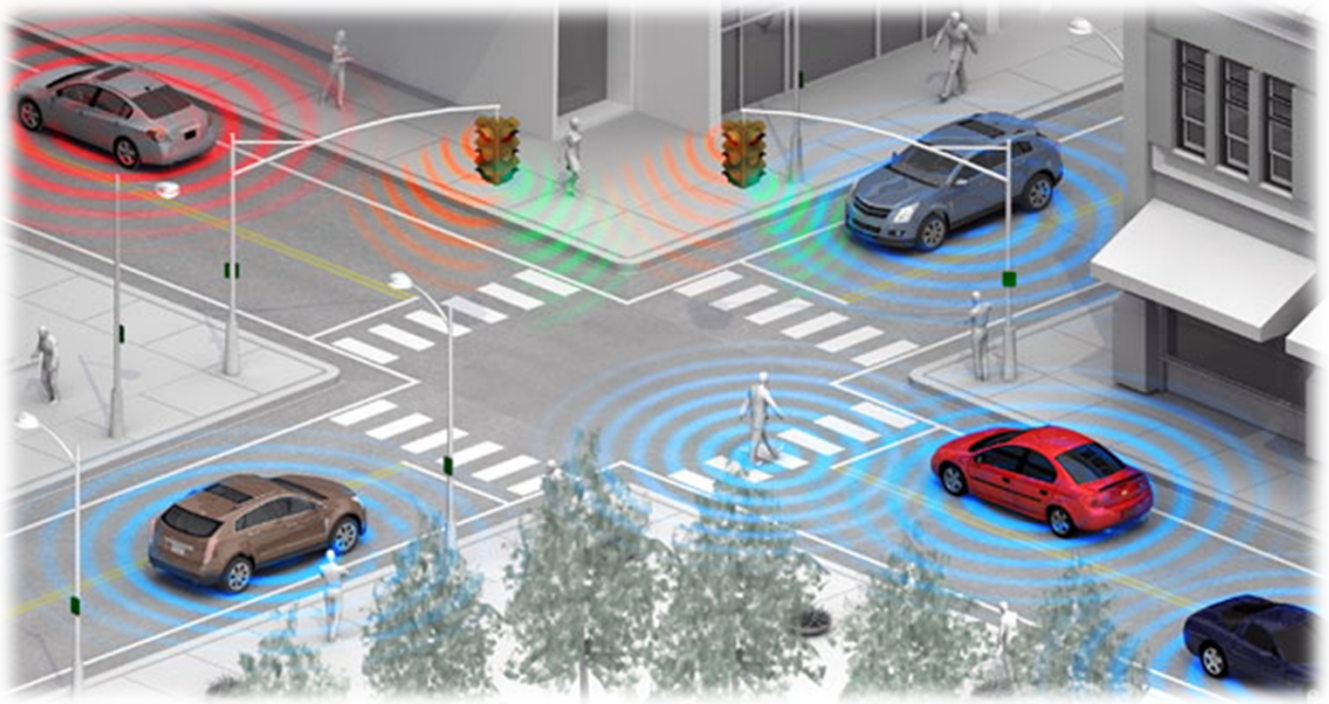
[1] imec, Leuven, Belgium

[2] Vrije Universiteit Brussel, Belgium

A mm-wave sensor on a fingertip...

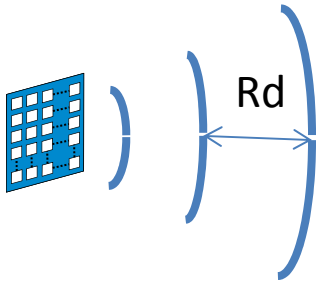


Short range radars
Boosting road safety



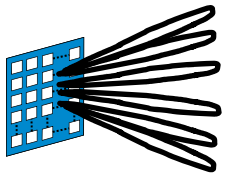
Focus on person detection

Turning application requirements into specifications



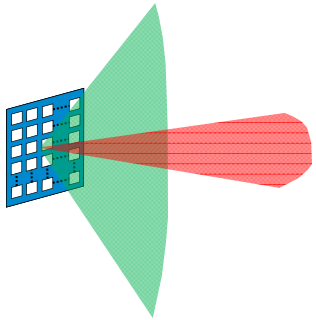
10cm depth resolution

bandwidth larger than 1.5GHz



1deg azimuth angular resolution

antenna aperture and # elements



160deg field of view

no directive antennas

[Hasch, MTT12]

A 28nm CMOS 79GHz Radar TX
Outline

PRN coded architecture

Digital intensive

CMOS 79GHz design

Robustness

Measurement results

High performance

A 28nm CMOS 79GHz Radar TX
Outline

PRN coded architecture

Digital intensive

CMOS 79GHz design

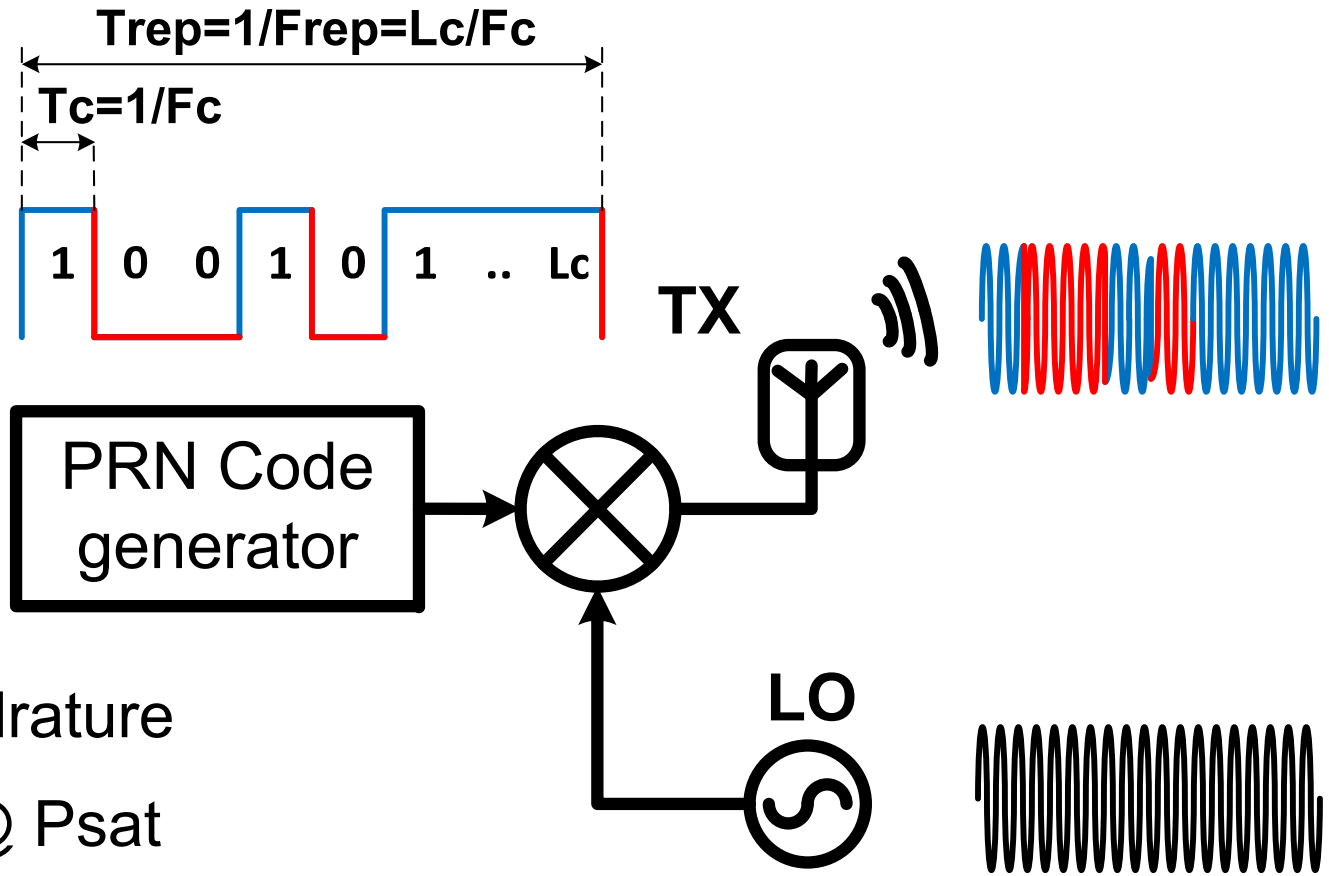
Robustness

Measurement results

High performance

PRN coded CW radars

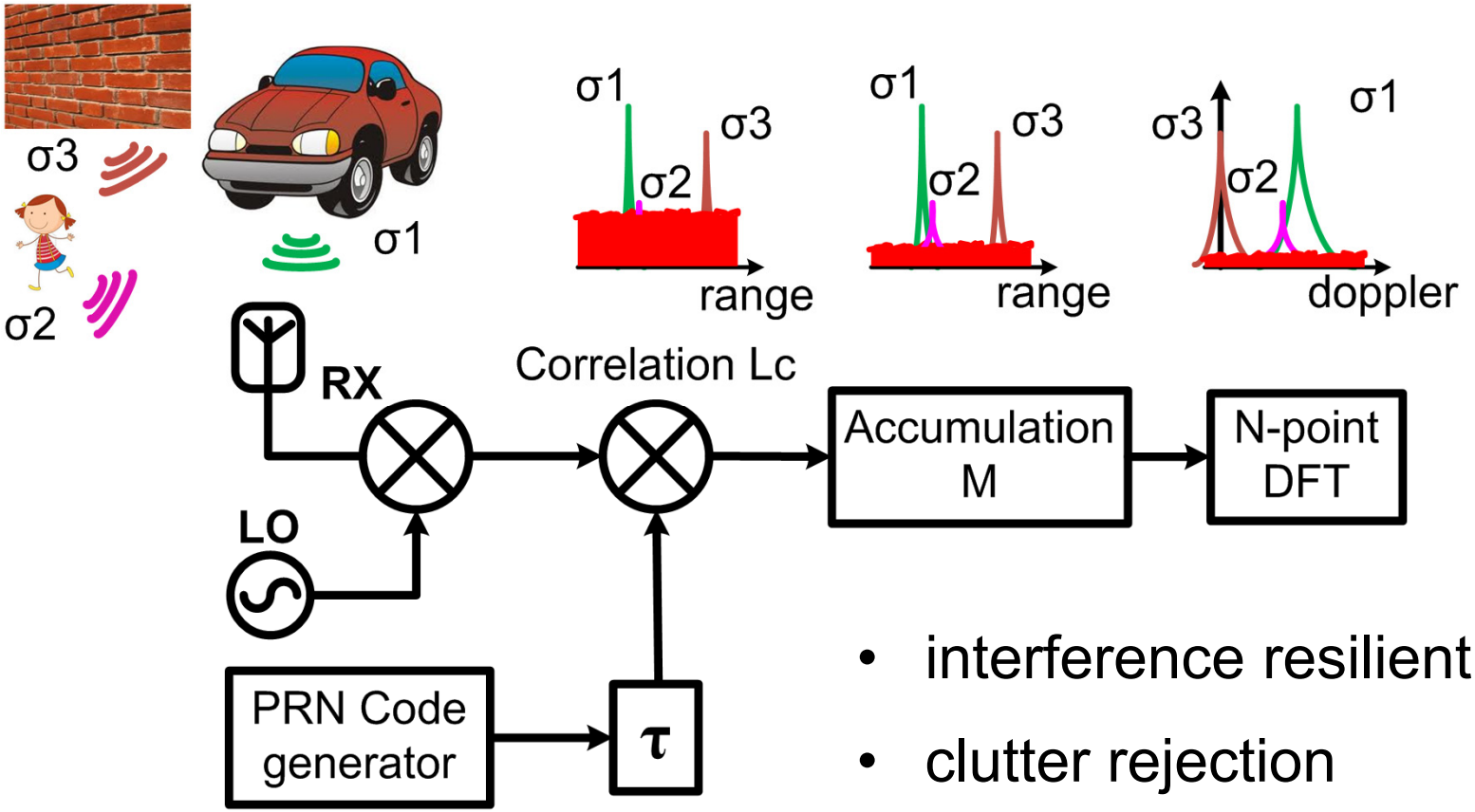
A simple transmitter



- no LO quadrature
- transmits @ Psat
- code domain MIMO possible

PRN coded CW radars

A digital intensive receiver



- interference resilient
- clutter rejection

Link-Budget for 4 TX + 4 RX

25m range possible in detection mode

Parameters:

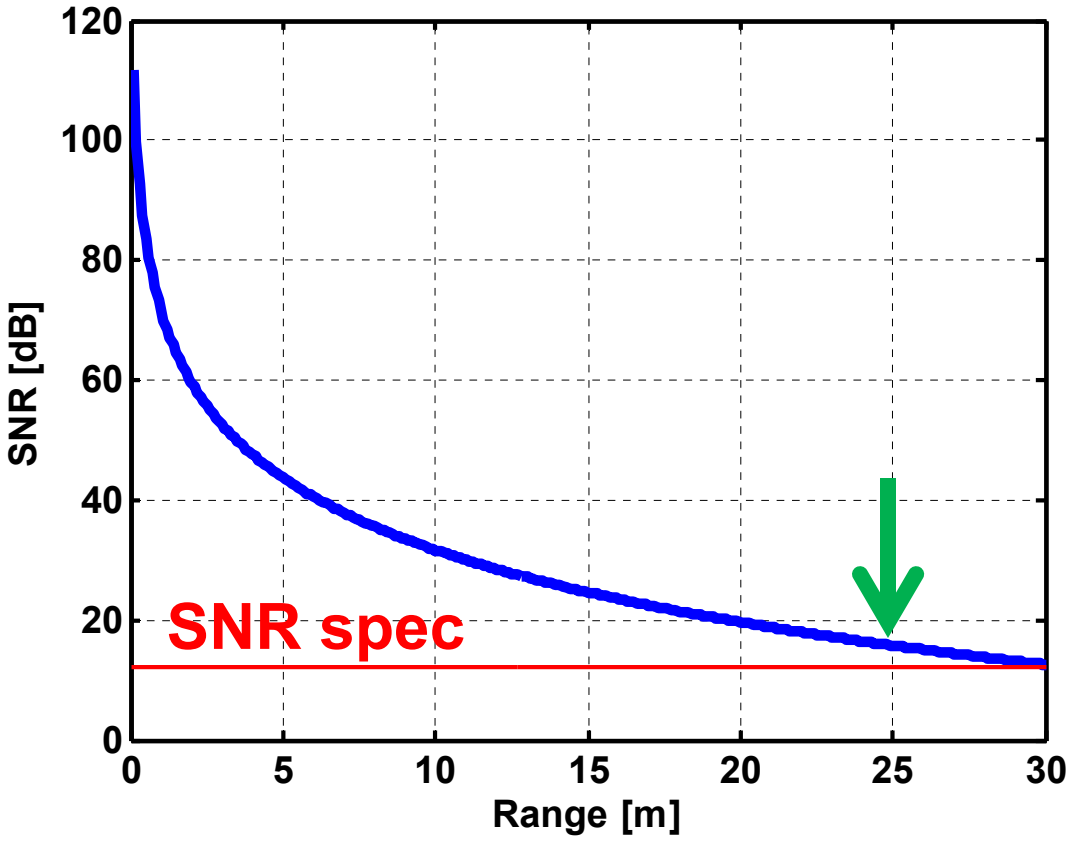
Po=+10dBm

Fc=2Gsps

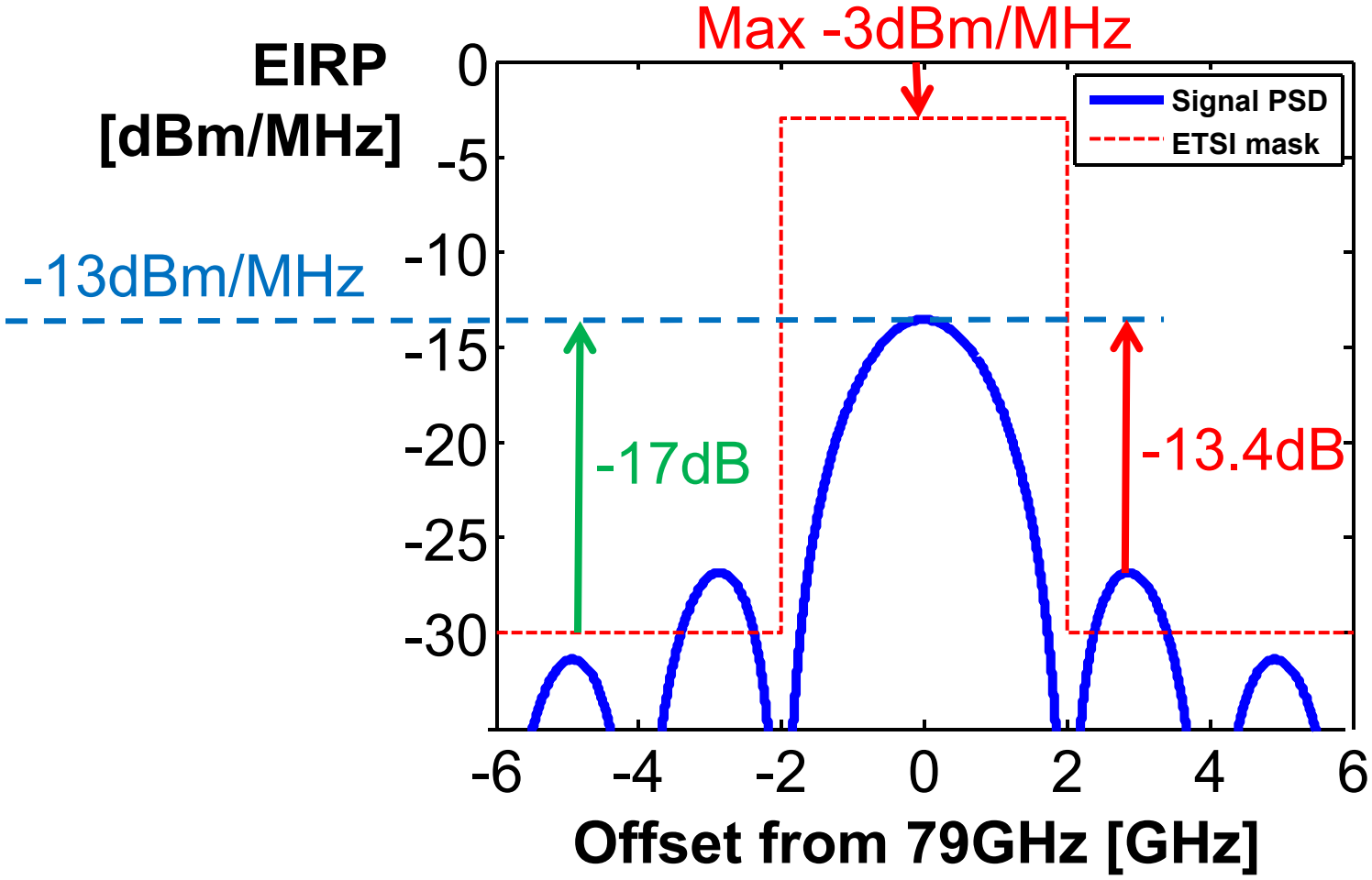
NF=6dB

Lc=511

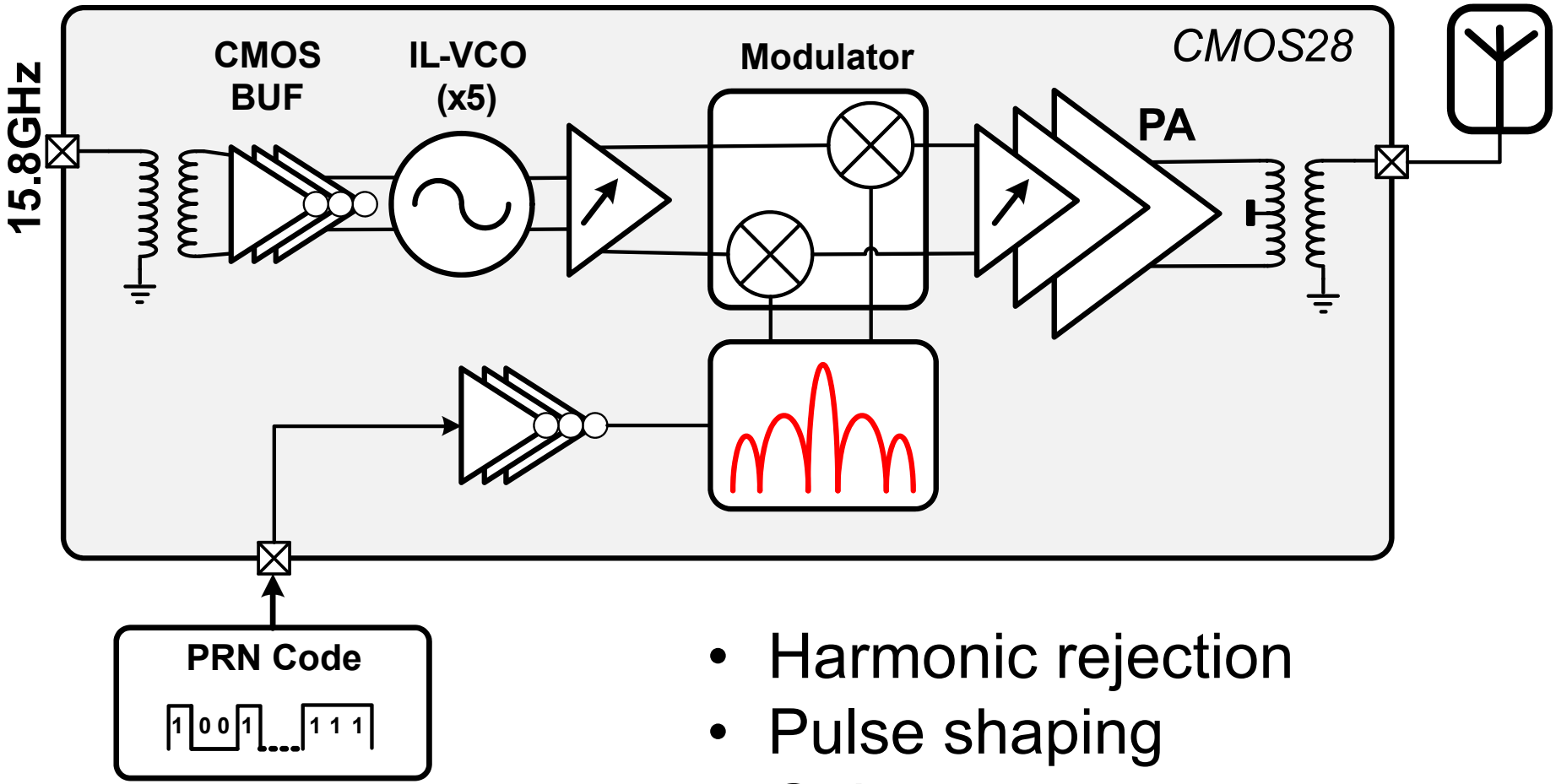
M=1024



BPSK frequency side-lobes
At least -17dBc needed!



Our TX reduces frequency side lobes



- Harmonic rejection
- Pulse shaping
- Gain control

A 28nm CMOS 79GHz Radar TX
Outline

PRN coded architecture

Digital intensive

CMOS 79GHz design

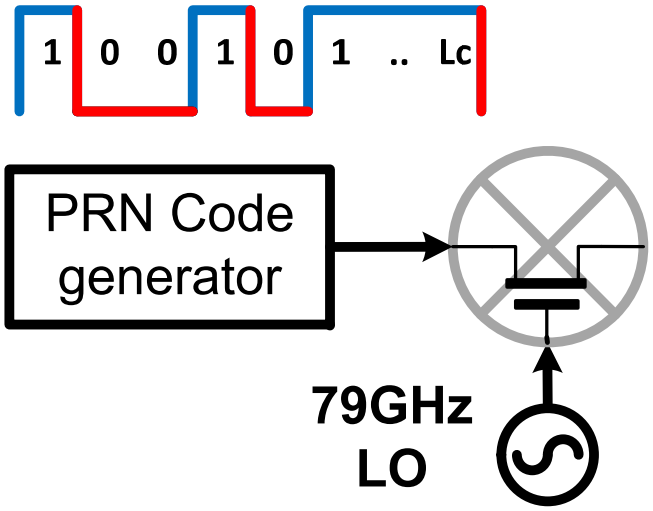
Robustness

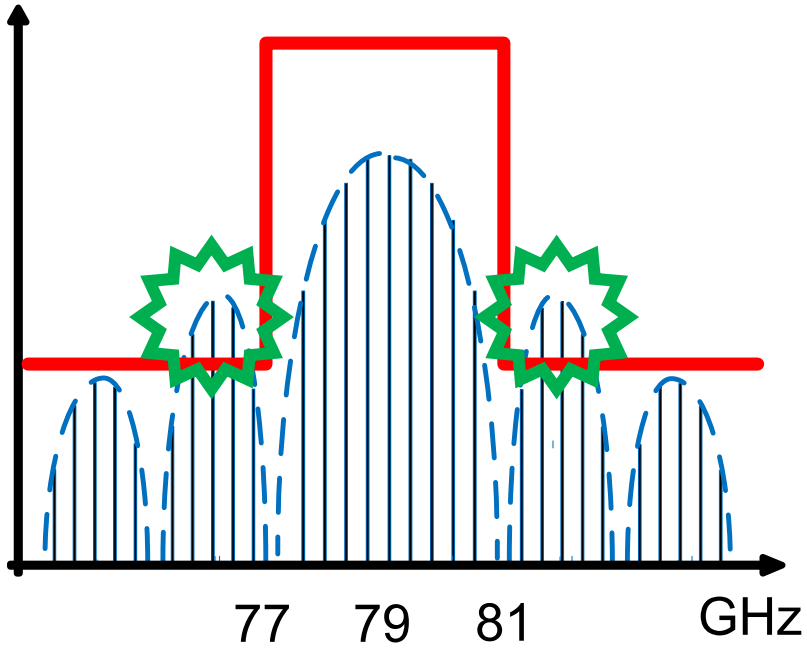
Measurement results

High performance

79GHz Phase-Modulator

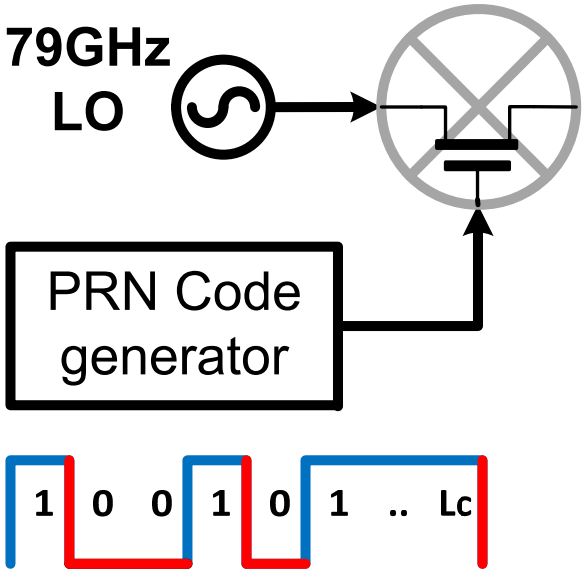
linear BB x non-linear LO

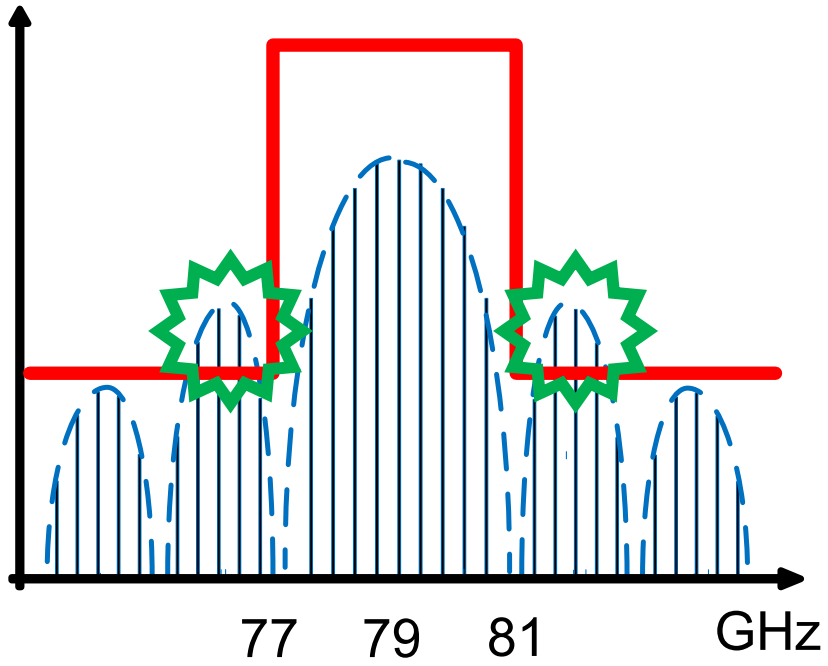




- Passive mixing possible
- Power consuming 79GHz LO buffers

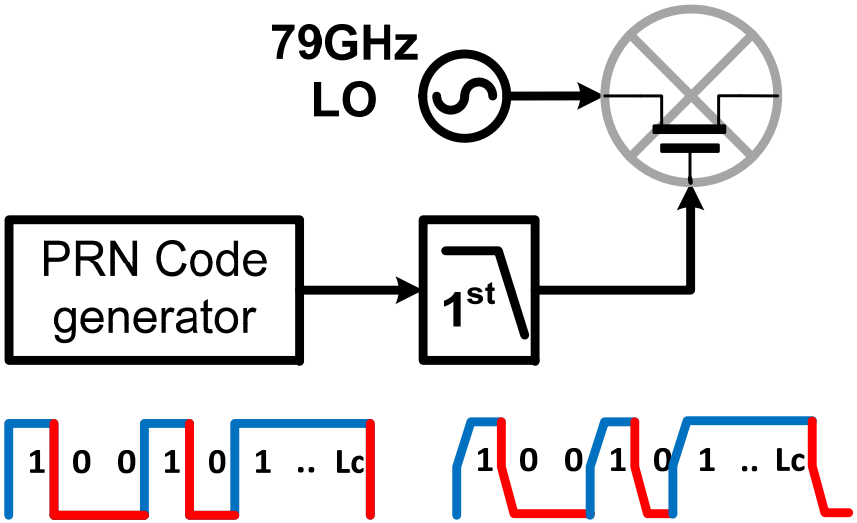
79GHz Phase-Modulator
linear LO x non-linear BB

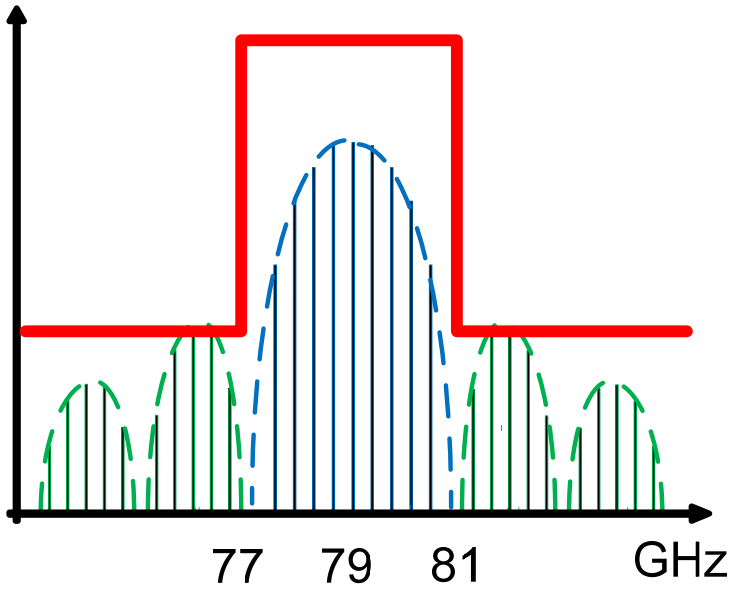




- lower 79GHz swing and so less power
- full swing PRN code drives nicely a gate
- But gain control needed

79GHz Phase-Modulator
filtering a 2Gsps PRN baseband

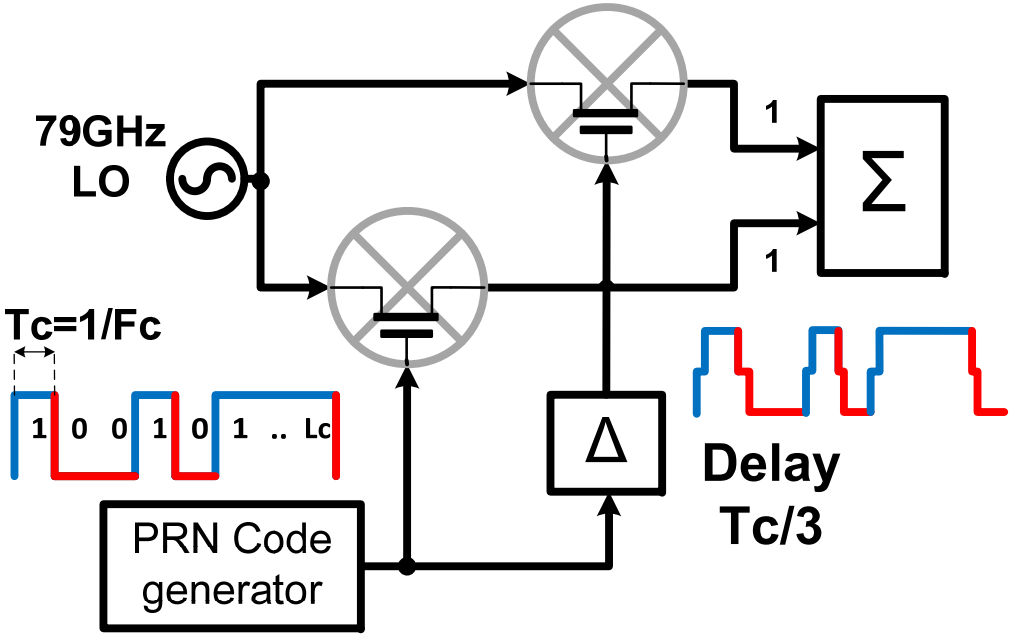


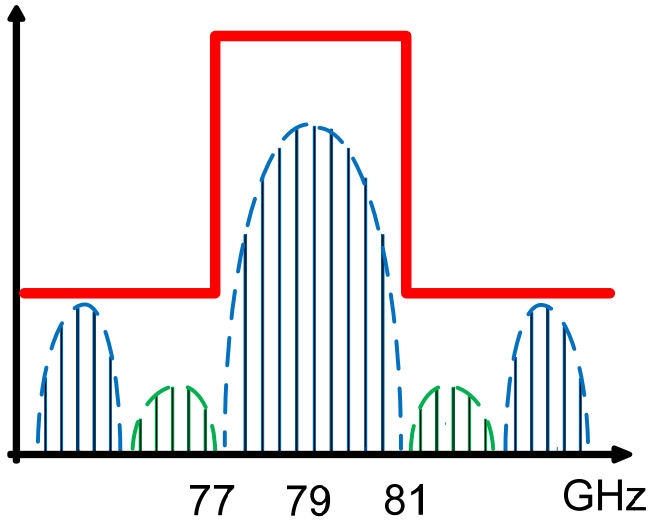


1st order LPF minimizes complexity

...but marginal in rejecting the closest 3rd order lobe

79GHz Phase-Modulator
harmonic rejection using delay line

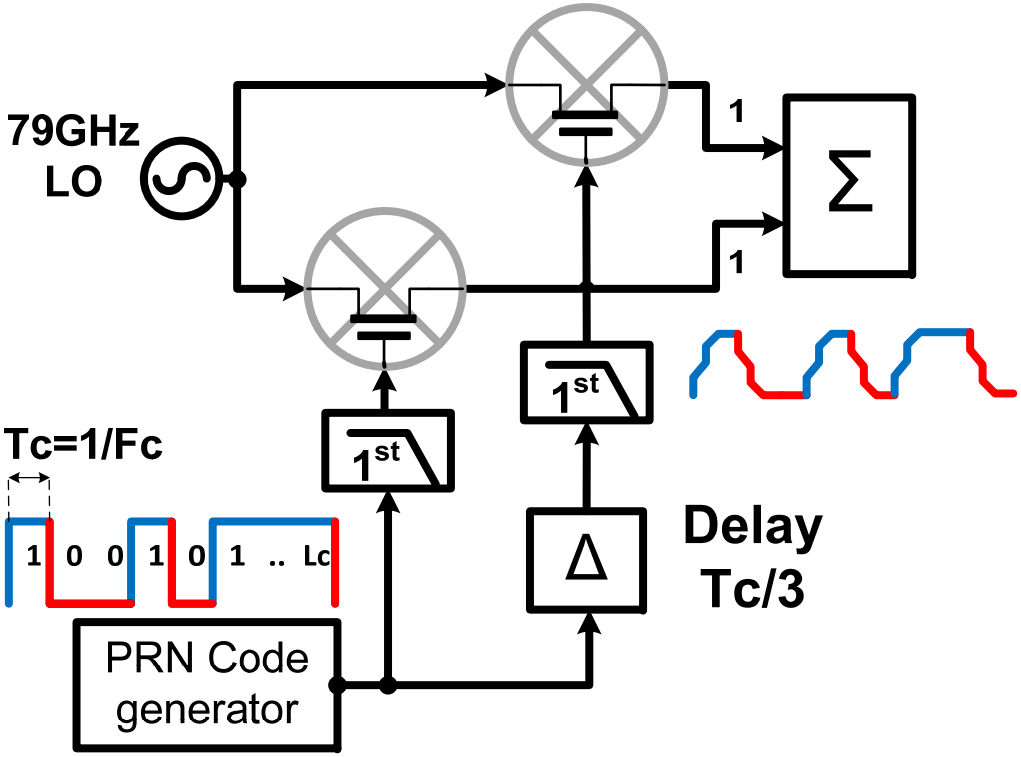


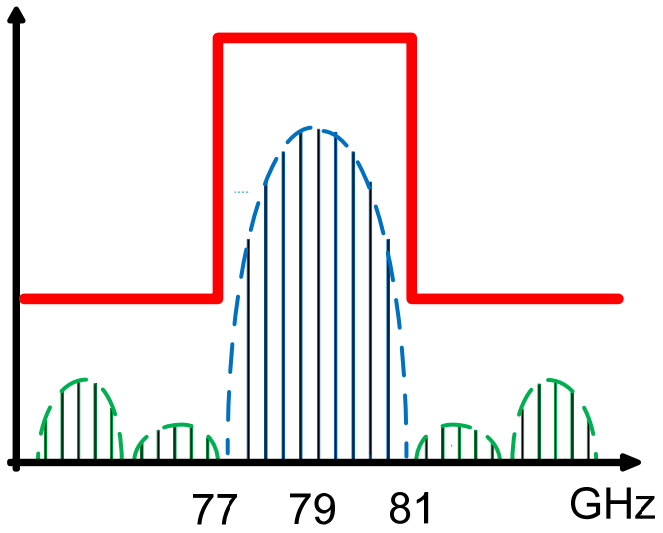


- Split mixer fed by delayed inputs and weighted sum
- Calibrated delay line

Ideally, closest 3rd order lobe strongly rejected

79GHz Phase-Modulator
harmonic rejection & LPF

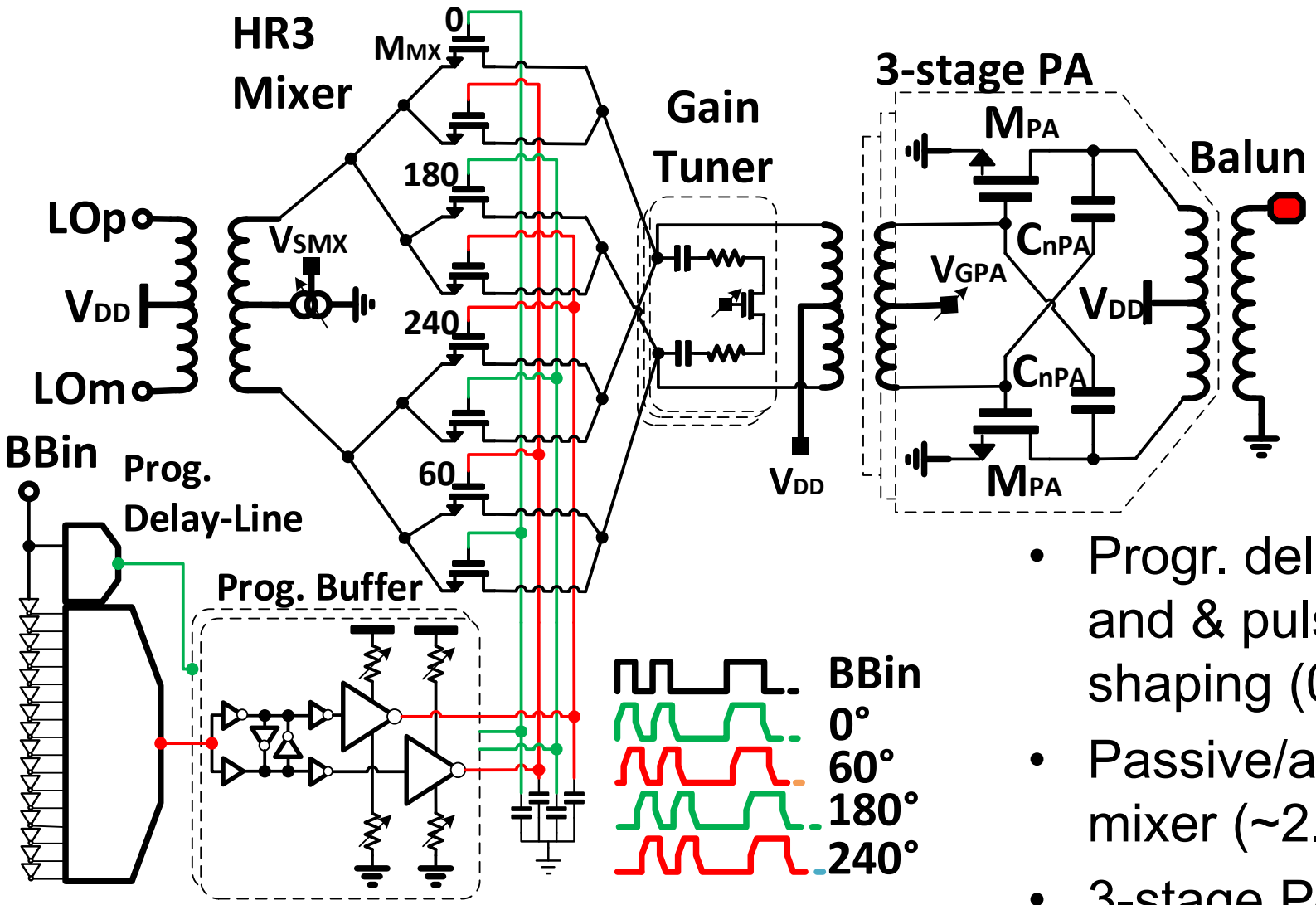




Pulse shaping after delaying

Most effective side-lobes rejection @ lowest cost

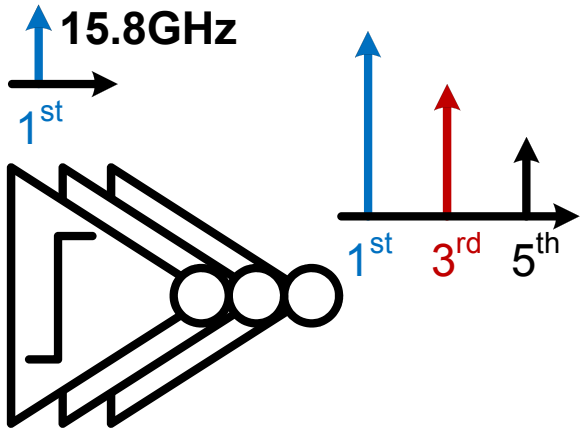
79GHz Modulator & PA schematic



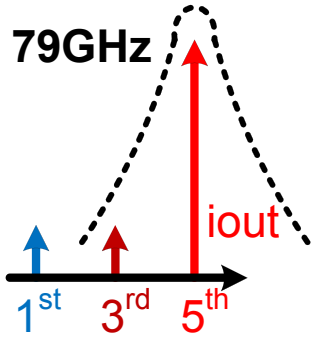
- Progr. delay line and & pulse shaping (0.9mW)
- Passive/active mixer (~2.7mW)
- 3-stage PA (88mW)

5x subharmonic injection locking

Boosting the injected current

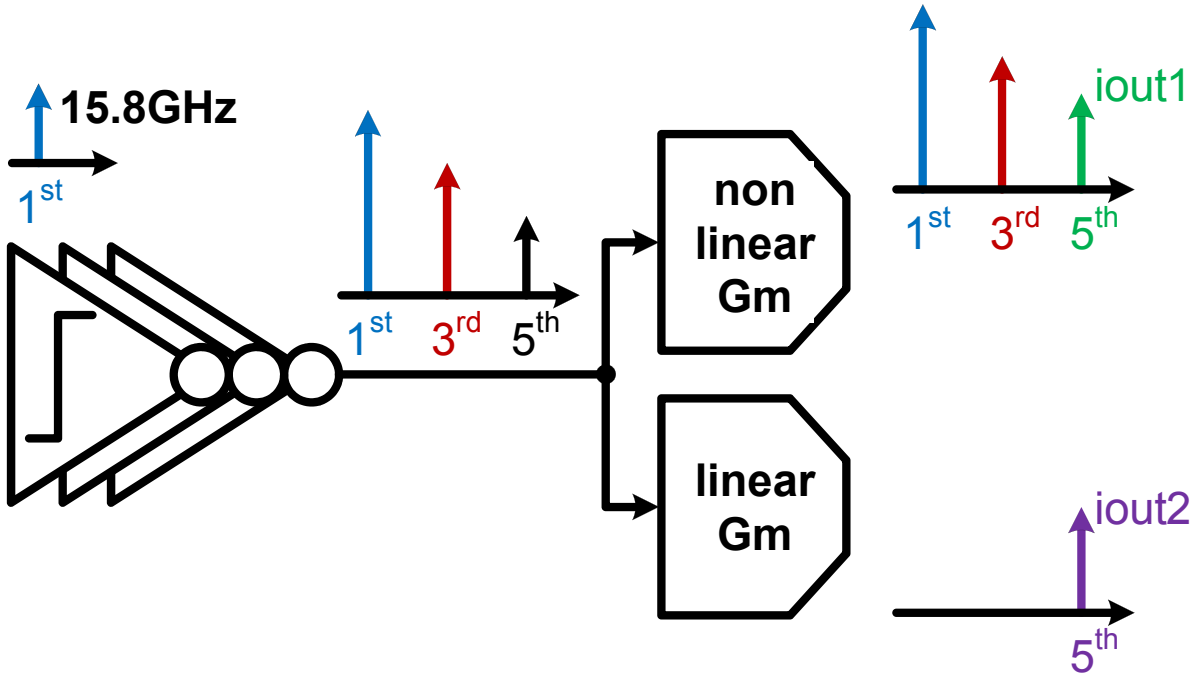


$$Locking\ range = \frac{\omega_0}{2 \cdot Q} \cdot \frac{I_{inj}}{I_{osc}}$$

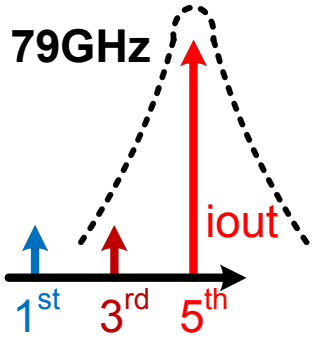


5x subharmonic injection locking

Boosting the injected current

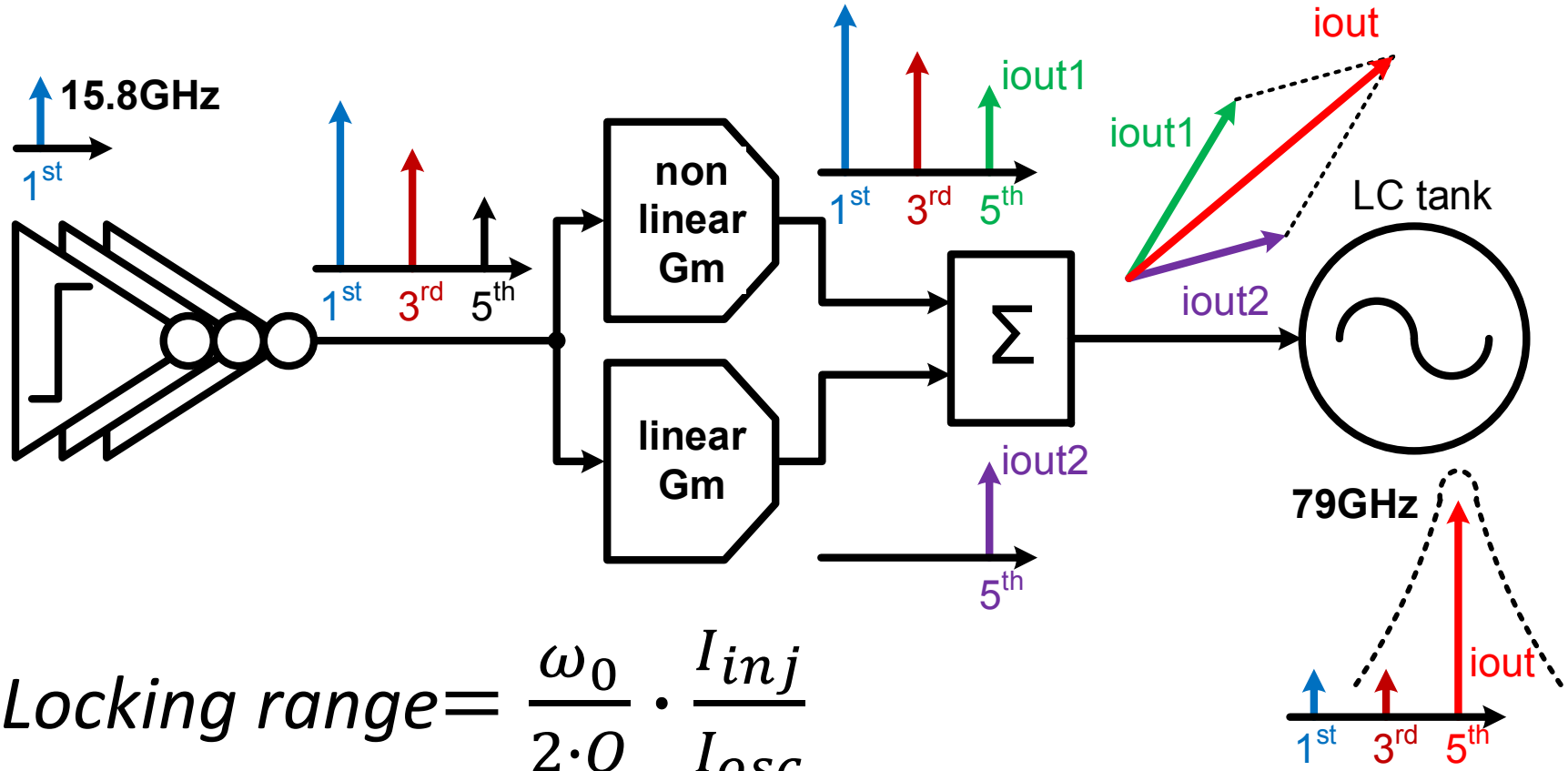


$$Locking\ range = \frac{\omega_0}{2 \cdot Q} \cdot \frac{I_{inj}}{I_{osc}}$$



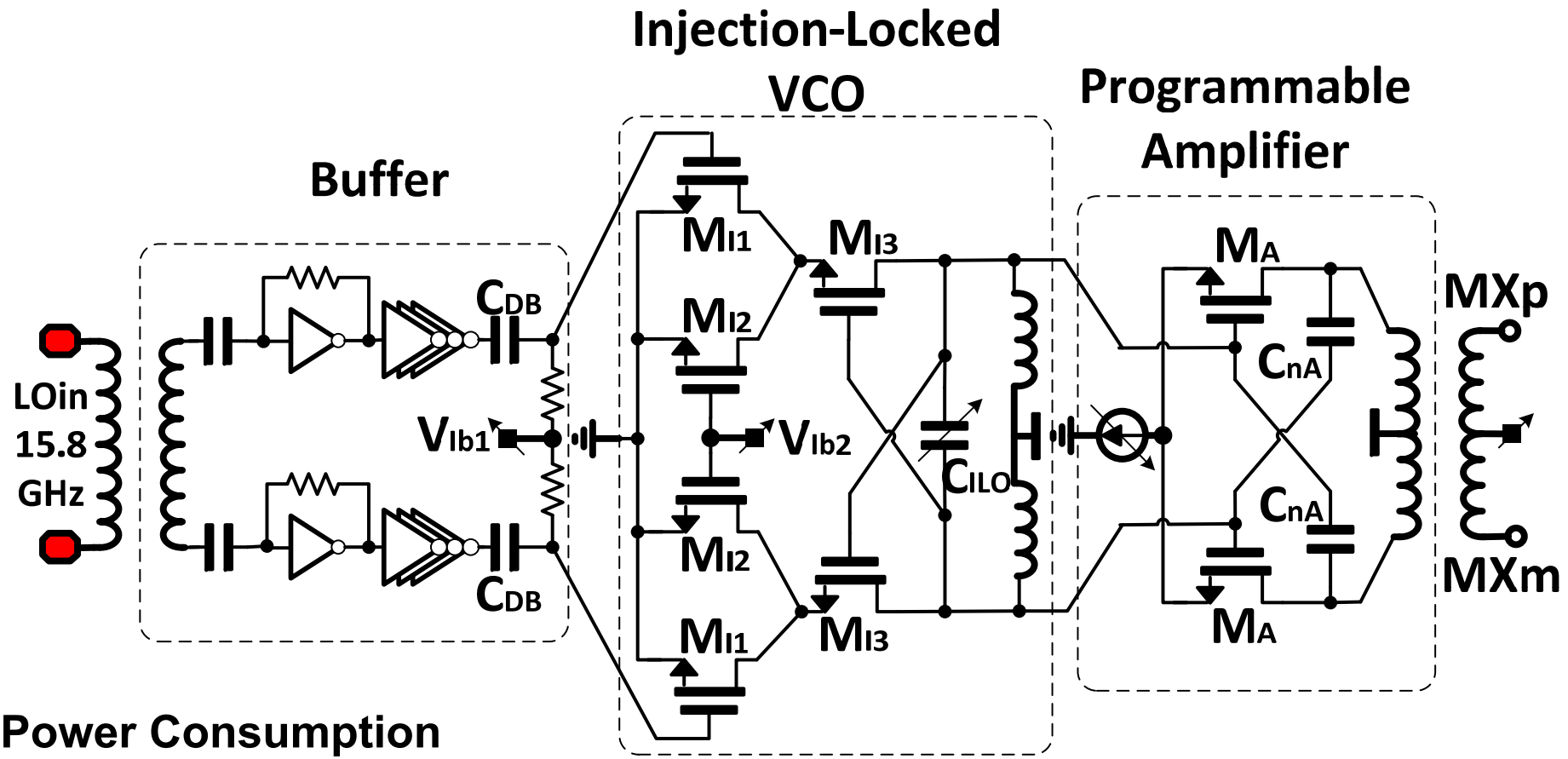
5x subharmonic injection locking

Boosting the injected current



$$Locking\ range = \frac{\omega_0}{2 \cdot Q} \cdot \frac{I_{inj}}{I_{osc}}$$

Subharmonic injection locked VCO



Power Consumption

CMOS Buffer:	7mW
ILO VCO core:	7mW
Amplifier:	9mW

A 28nm CMOS 79GHz Radar TX
Outline

PRN coded architecture

Digital intensive

CMOS 79GHz design

Robustness

Measurement results

High performance

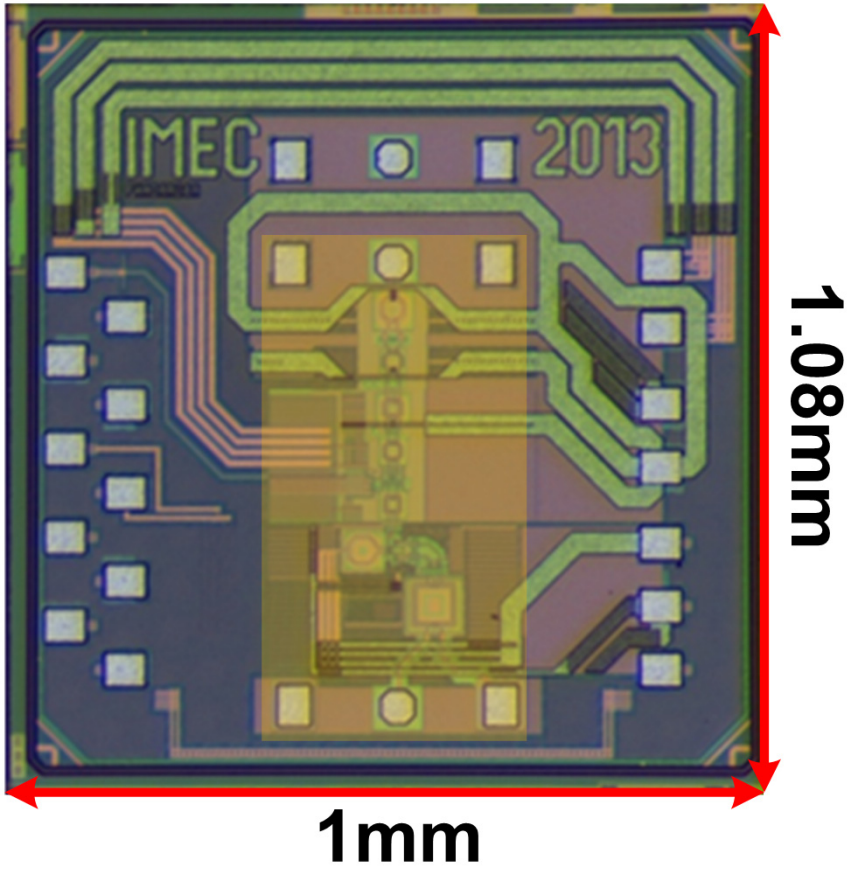
Chip micrograph

TX core area is 0.24 mm^2

28nm CMOS HPM

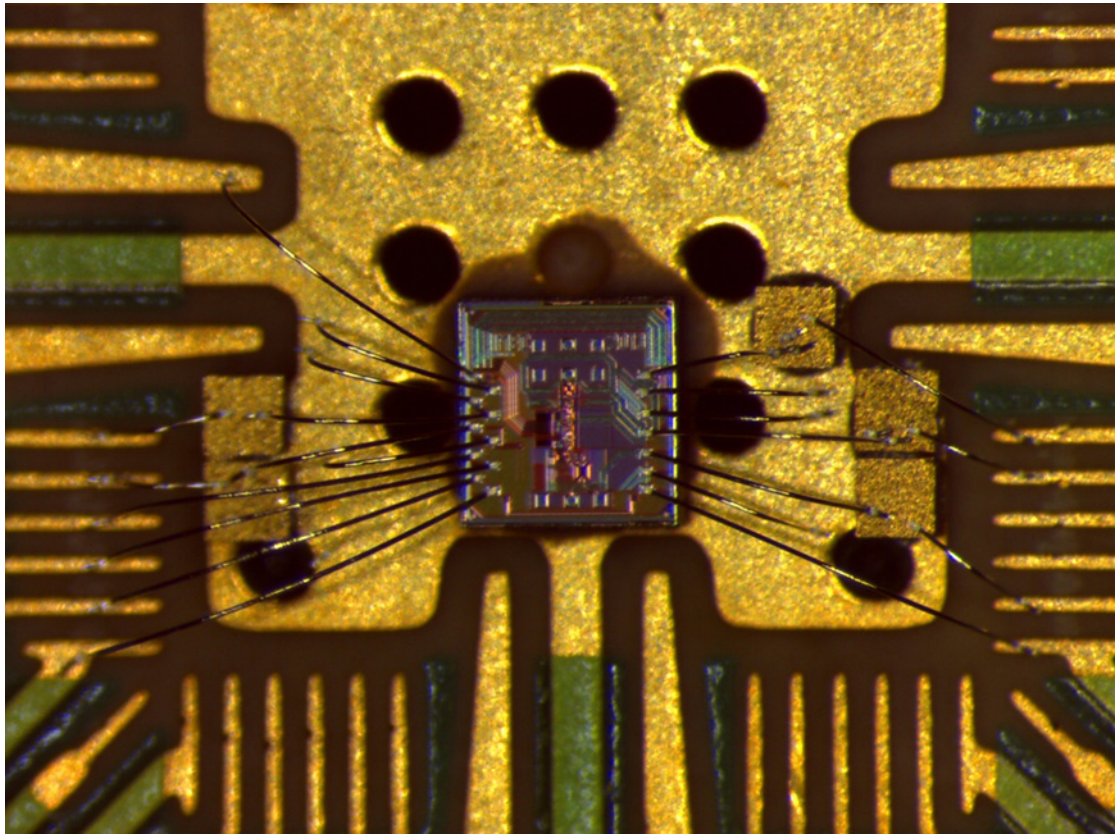
0.9V Core Supply

121mW @ 11dBm



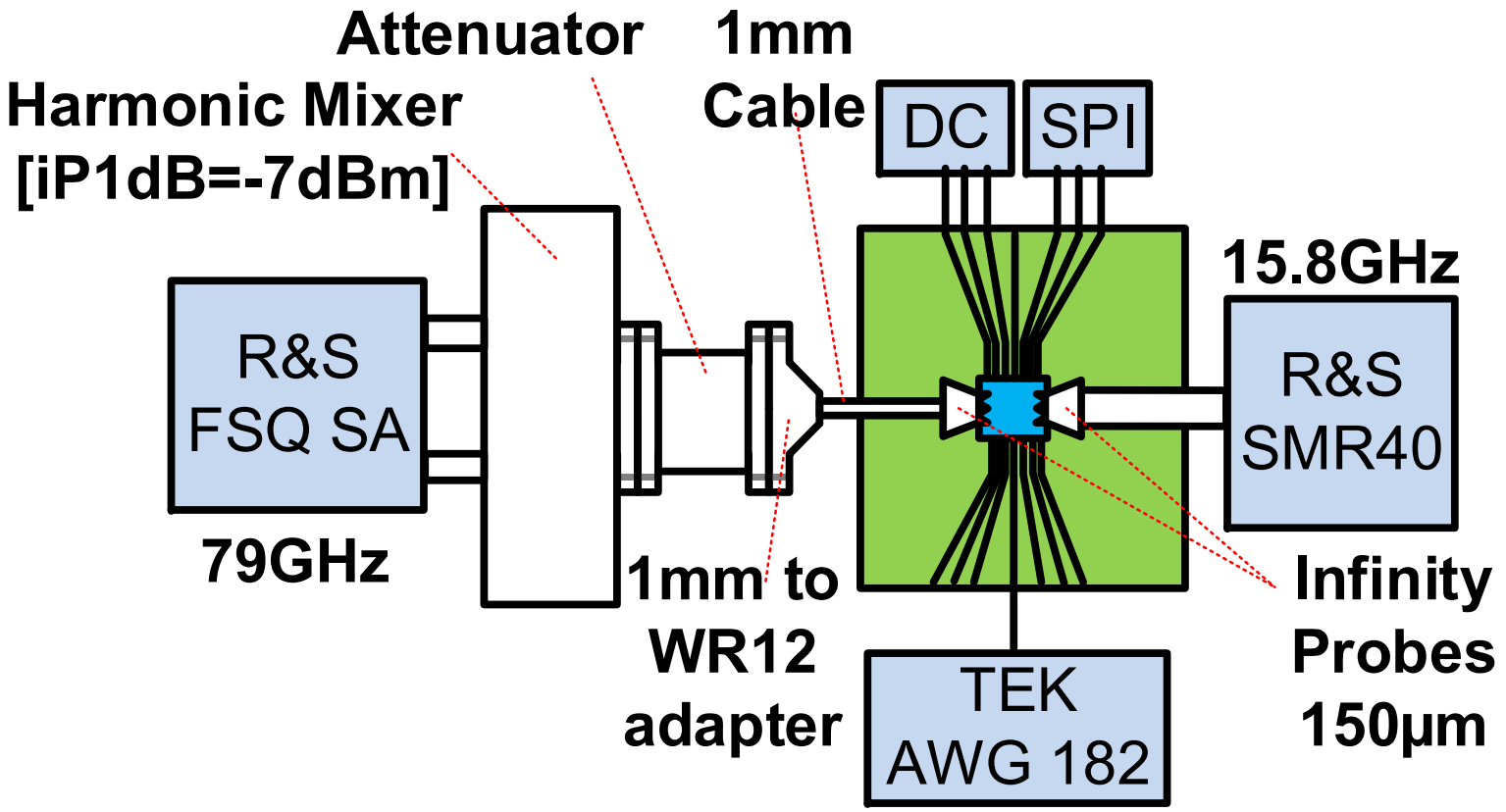
Measurement setup

DC & Digital IOs bonded



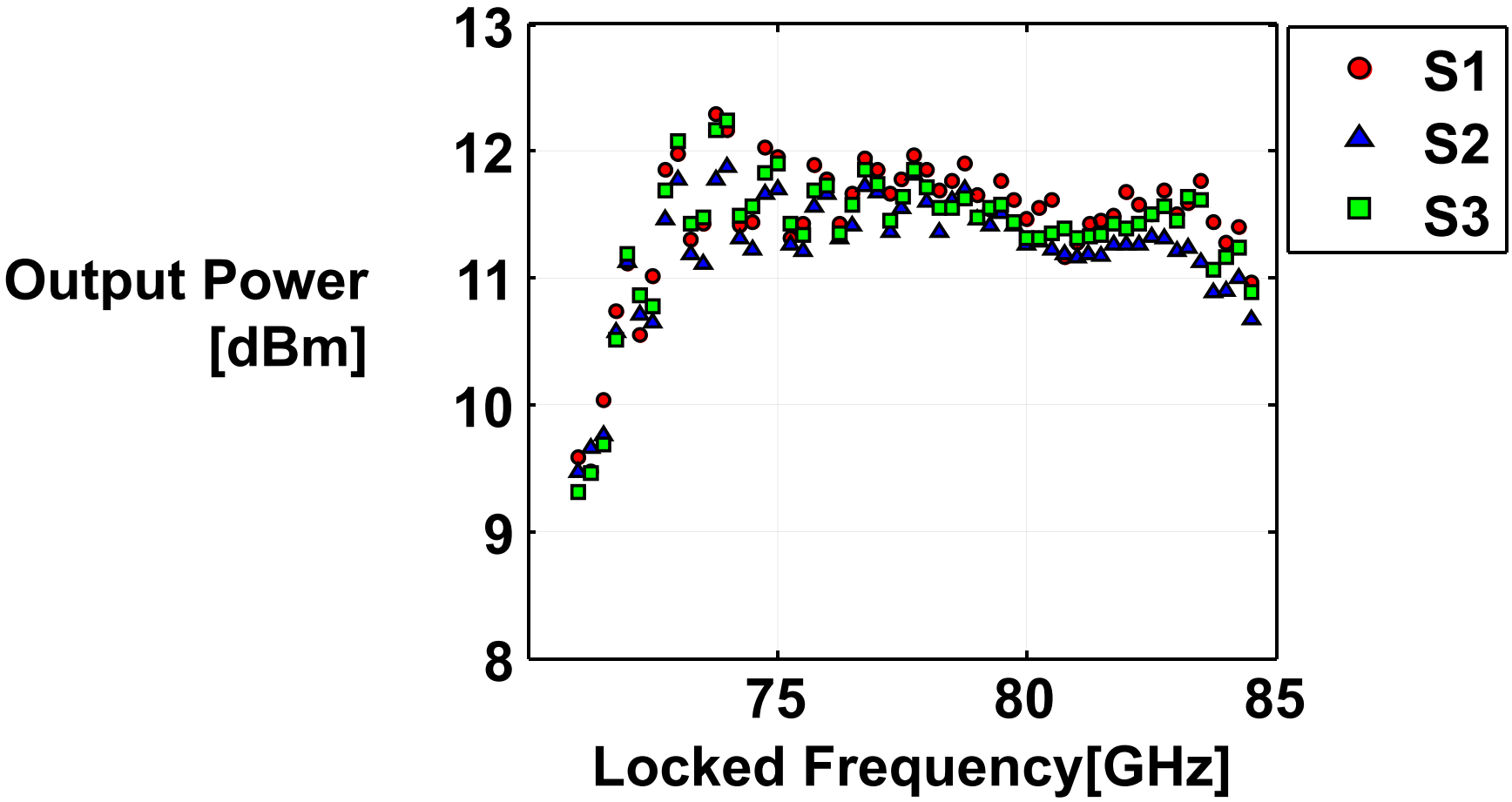
Measurement setup

Block diagram



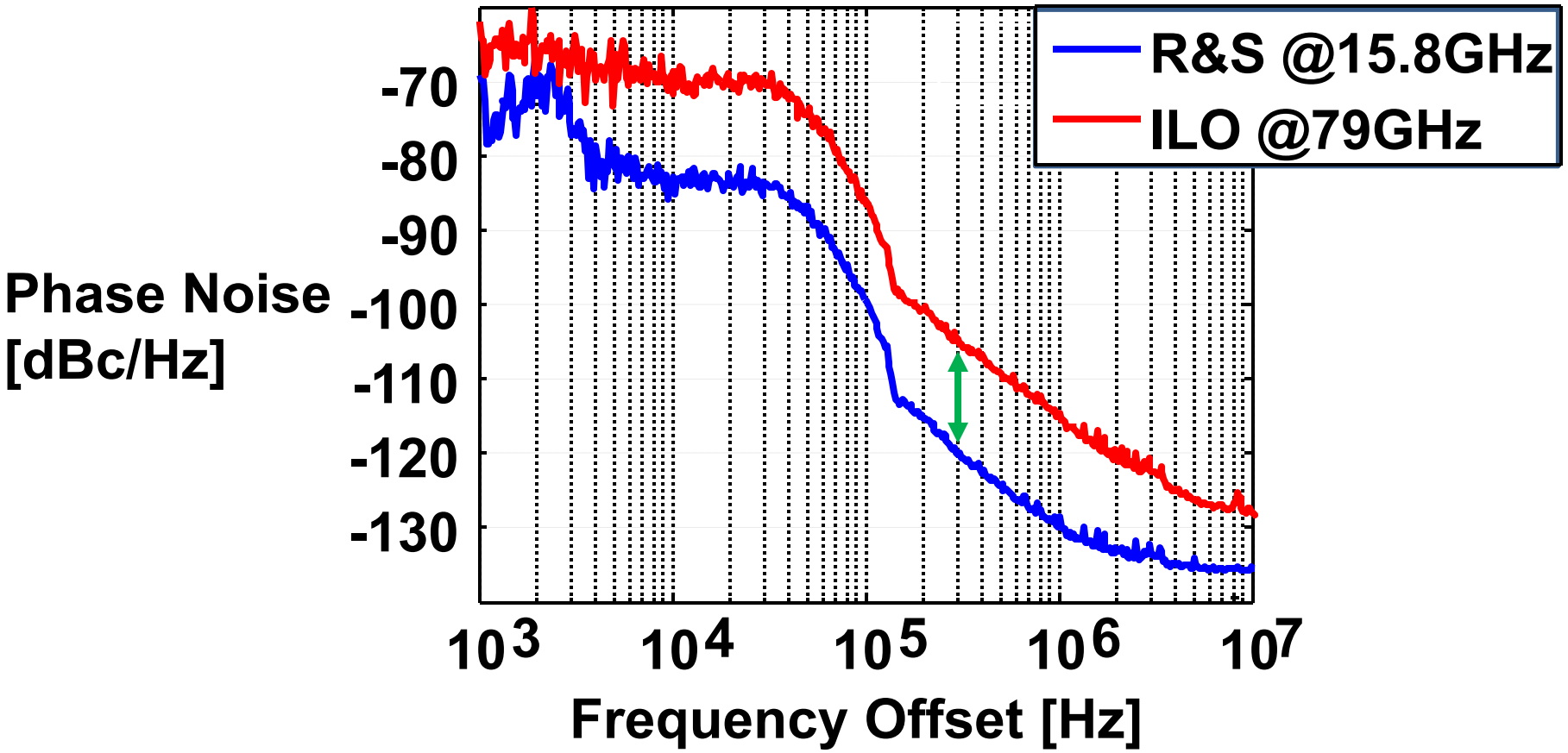
TX output power vs frequency

13GHz locked bandwidth

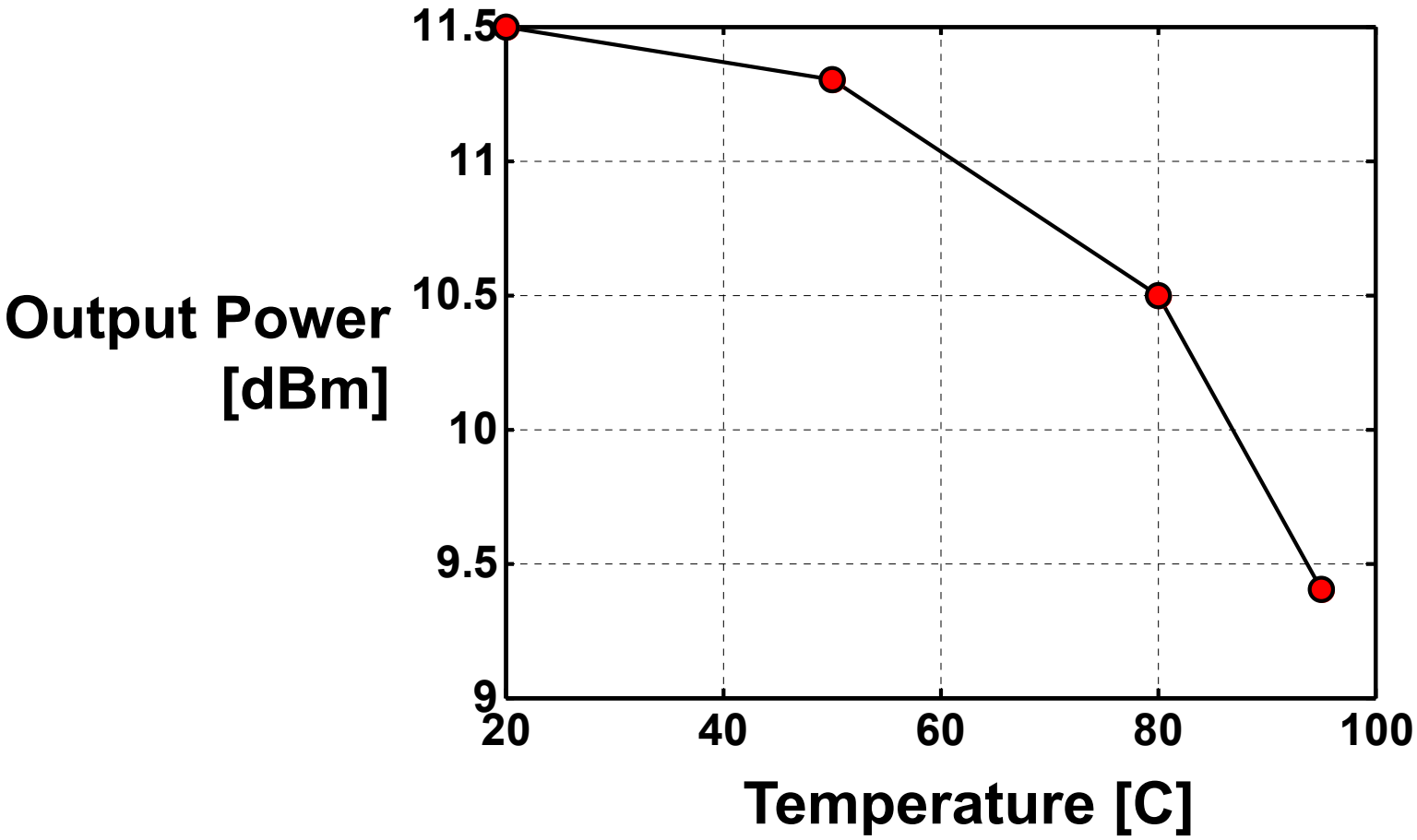


5x SH-ILO VCO phase noise

14dB delta from 15.8GHz input

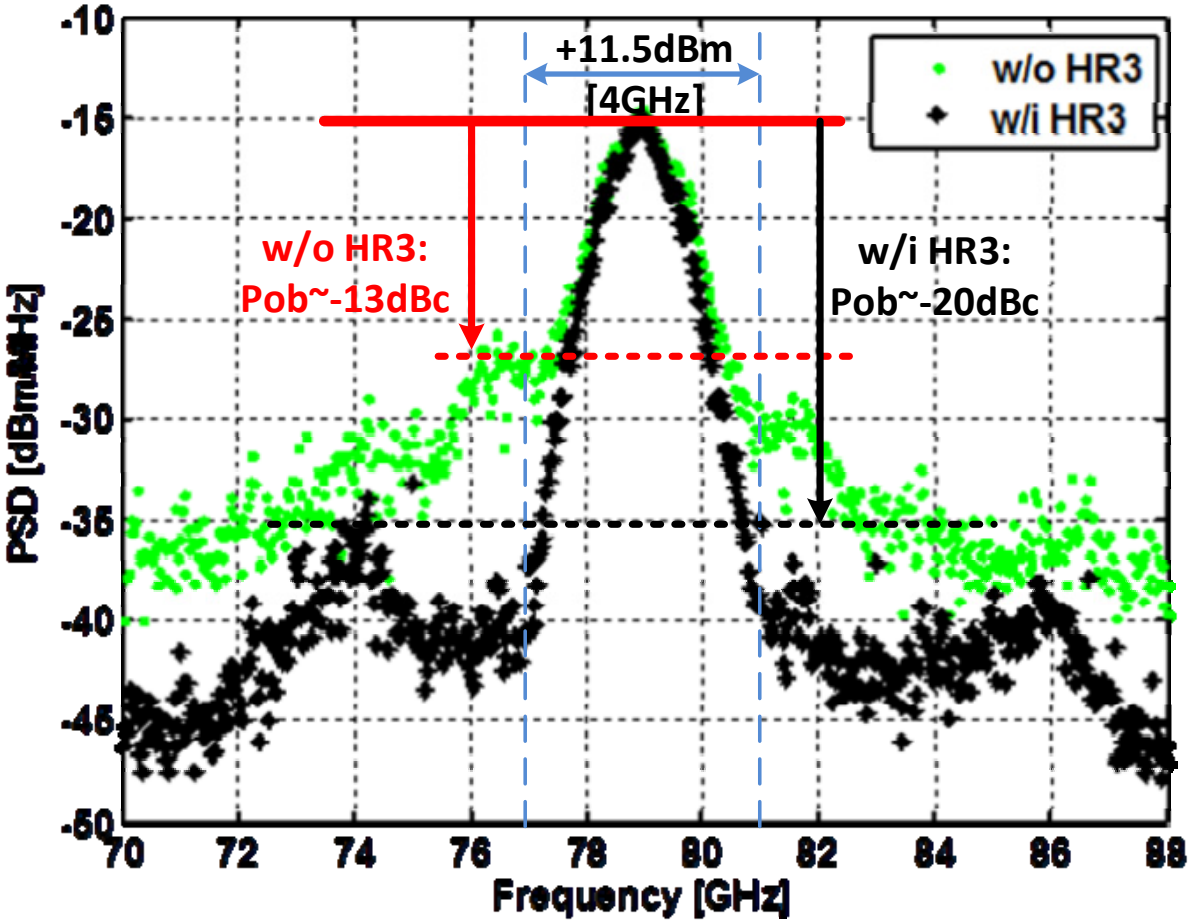


TX output power vs. temperature
measured with heated air-flow



TX PM spectrum @ 79GHz

2Gbps chip rate w/i & w/o HR3



1st CMOS PMCW 79GHz radar TX

Reference	Tech	VDD [V]	Radar	Fc [GHz]
[Kawano09]	CMOS90	1.2	FMCW	77
[Mitomo10]	CMOS90	1.2	FMCW	77
[Lee10]	CMOS65	1.2	FMCW	77
[To11]	CMOS65	1	n/a	77/84
[Wu13]	CMOS65	1.2	FMCW	62
[Trotta07]	SiGe 200G	5.5	PMCW	79
[Ragonese09]	SiGe 230G	2.5	PMCW	24
THIS WORK	**CMOS28**	**0.9**	**PMCW**	**77/79**

7cm depth resolution @ 2Gbps

Reference	Tech	VDD [V]	Radar	Fc [GHz]	BW [GHz]
[Kawano09]	CMOS90	1.2	FMCW	77	0.2
[Mitomo10]	CMOS90	1.2	FMCW	77	0.6
[Lee10]	CMOS65	1.2	FMCW	77	0.7
[To11]	CMOS65	1	n/a	77/84	n/a
[Wu13]	CMOS65	1.2	FMCW	62	1.2
[Trotta07]	SiGe 200G	5.5	PMCW	79	1.235
[Ragonese09]	SiGe 230G	2.5	PMCW	24	2.1
THIS WORK	**CMOS28**	**0.9**	**PMCW**	**77/79**	**2**

Best reported TX efficiency

Reference	Tech	VDD [V]	Radar	Fc [GHz]	BW [GHz]	Pout [dBm]	Pdc [mW]	TX eff [%]
[Kawano09]	CMOS90	1.2	FMCW	77	0.2	6.3	660	0.6
[Mitomo10]	CMOS90	1.2	FMCW	77	0.6	-2.8	406	0.13
[Lee10]	CMOS65	1.2	FMCW	77	0.7	5.1	188	1.7
[To11]	CMOS65	1	n/a	77/84	n/a	13.5	420	5.3
[Wu13]	CMOS65	1.2	FMCW	62	1.2	5	89	3.5
[Trotta07]	SiGe 200G	5.5	PMCW	79	1.235	1.5	4100	0.03
[Ragonese09]	SiGe 230G	2.5	PMCW	24	2.1	3	80	3.3
THIS WORK	**CMOS28**	**0.9**	**PMCW**	**77/79**	**2**	**>11**	**121**	**>10.4**

A 28nm CMOS 79GHz Radar TX

Conclusions

PRN coded architecture

7cm resolution

A 28nm CMOS 79GHz Radar TX
Conclusions

PRN coded architecture

7cm resolution

CMOS 79GHz design

HR3 and wide-locked RF BW

A 28nm CMOS 79GHz Radar TX
Conclusions

PRN coded architecture

7cm resolution

CMOS 79GHz design

HR3 and wide-locked RF BW

Measurement results

+11dBm, 10% efficiency

A 28nm CMOS 79GHz Radar TX
Conclusions

PRN coded architecture

7cm resolution

CMOS 79GHz design

HR3 and wide-locked RF BW

Measurement results

+11dBm, 10% efficiency

Future work: RX and packaging

A Push-Pull mm-Wave Power Amplifier with <0.8° AM-PM Distortion in 40nm CMOS

Shailesh Kulkarni, Prof. Patrick Reynaert

KU Leuven, ESAT-MICAS, Belgium

Outline

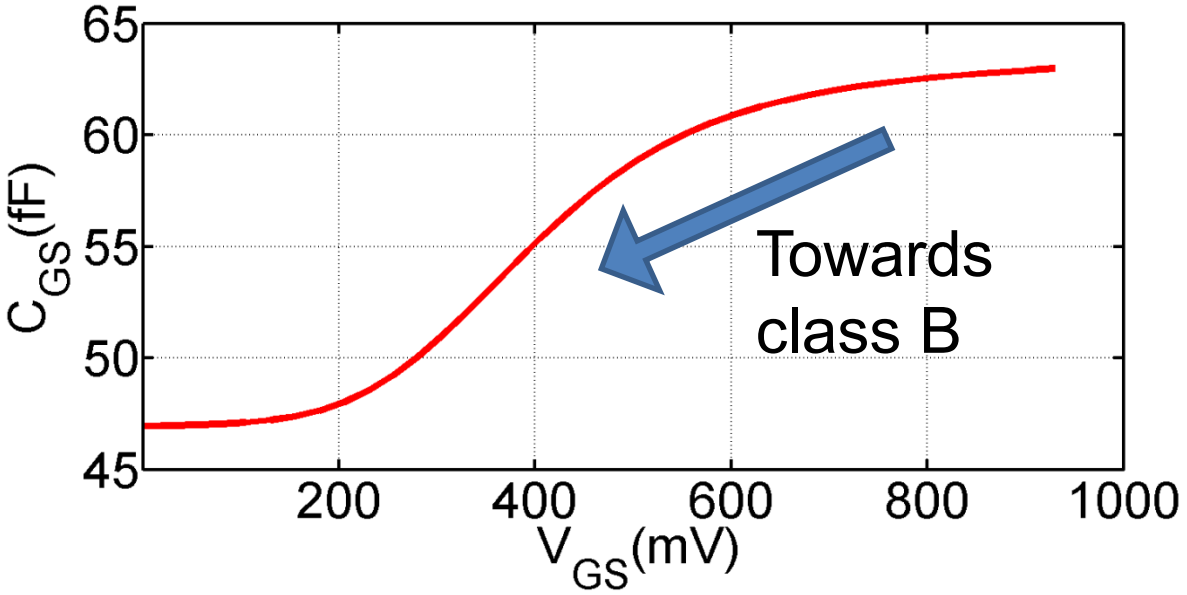
- Motivation
- Distortion source
- Architecture
- Measurements
- Conclusions

Motivation

- Mm-wave standards
  - Like 802.15.3c, 802.11ad at 60GHz
  - complex modulations (QAM-64)
  - complex PHY (OFDM)
- Large PAPR → linear PAs
- Efficiency
  - class A → class AB, class B
  - degradation in EVM, ACPR

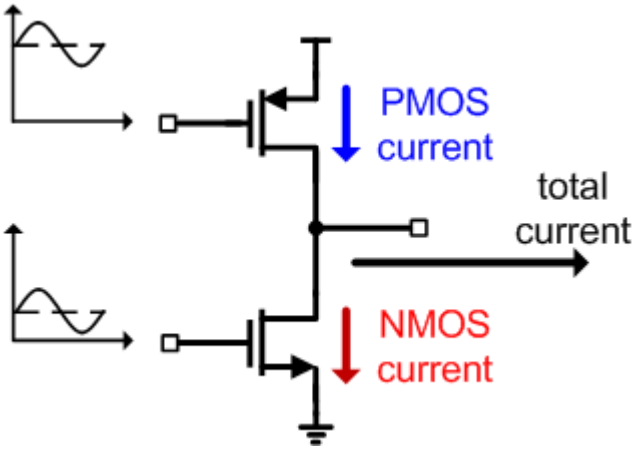
Distortion source

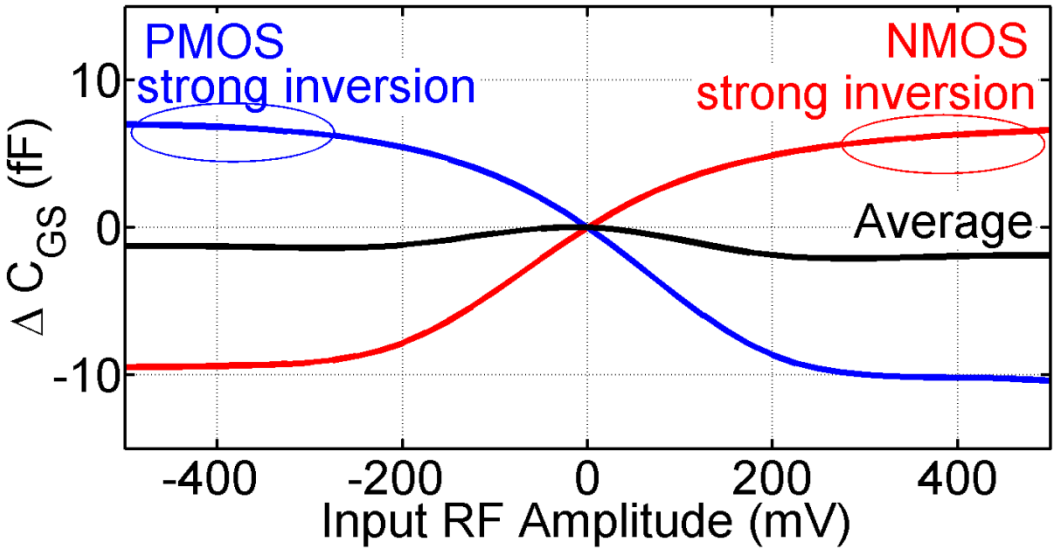
- Important source of the distortion
  - Biasing towards class B mode increases the AM-PM distortion
  - The non-linear input capacitance

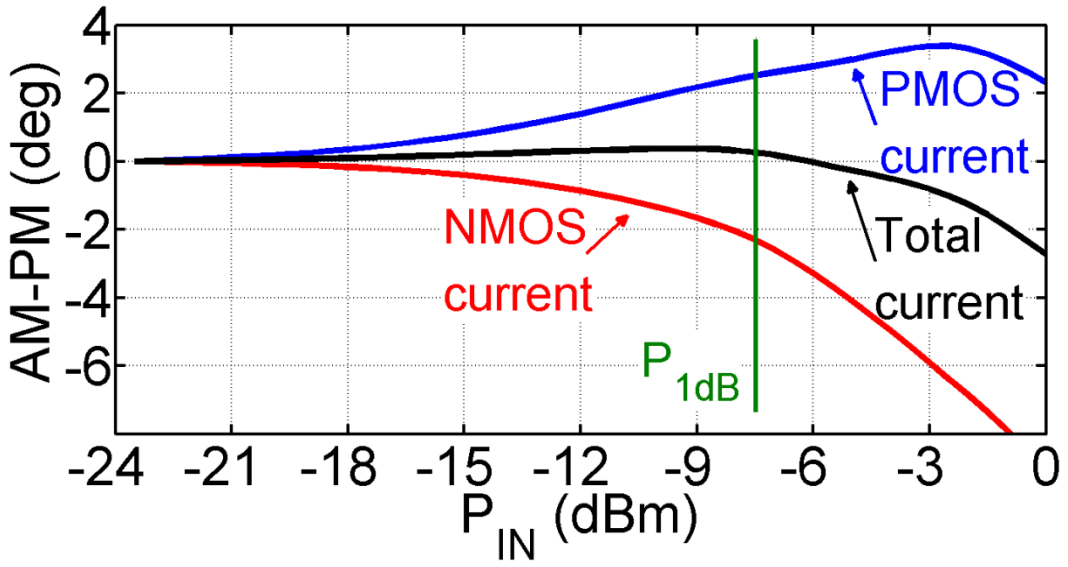


Proposed solution

- AM-PM cancellation
- PMOS
  - f_{MAX} >140GHz

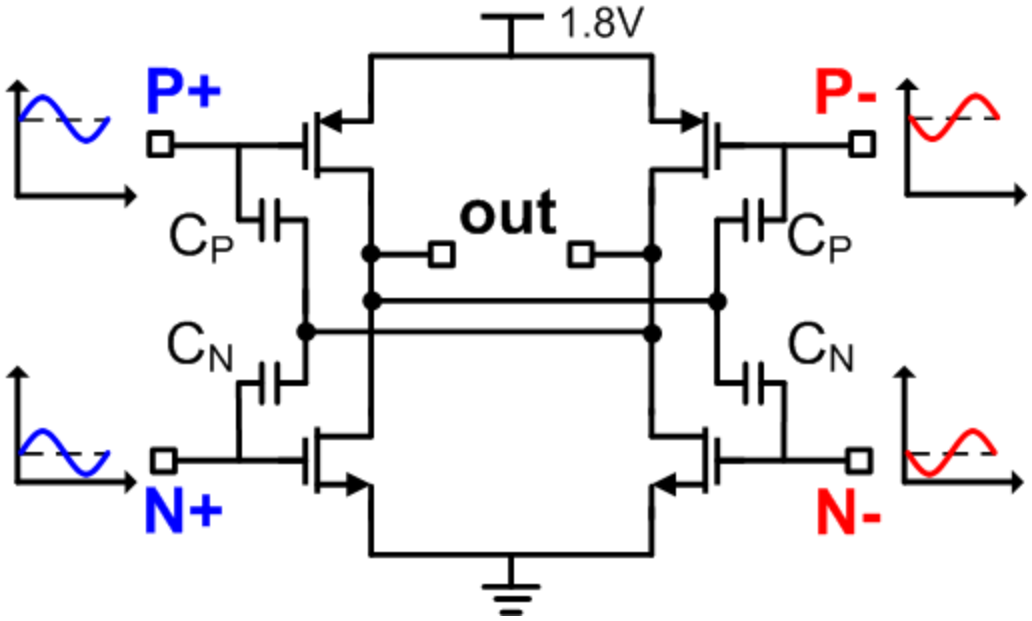


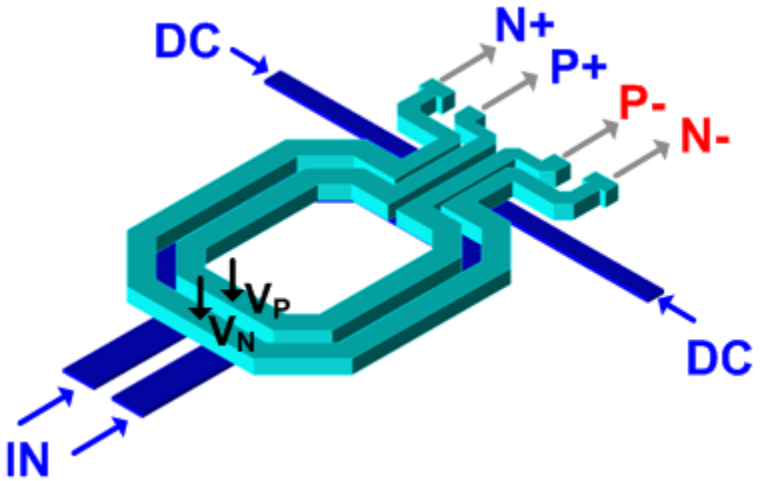




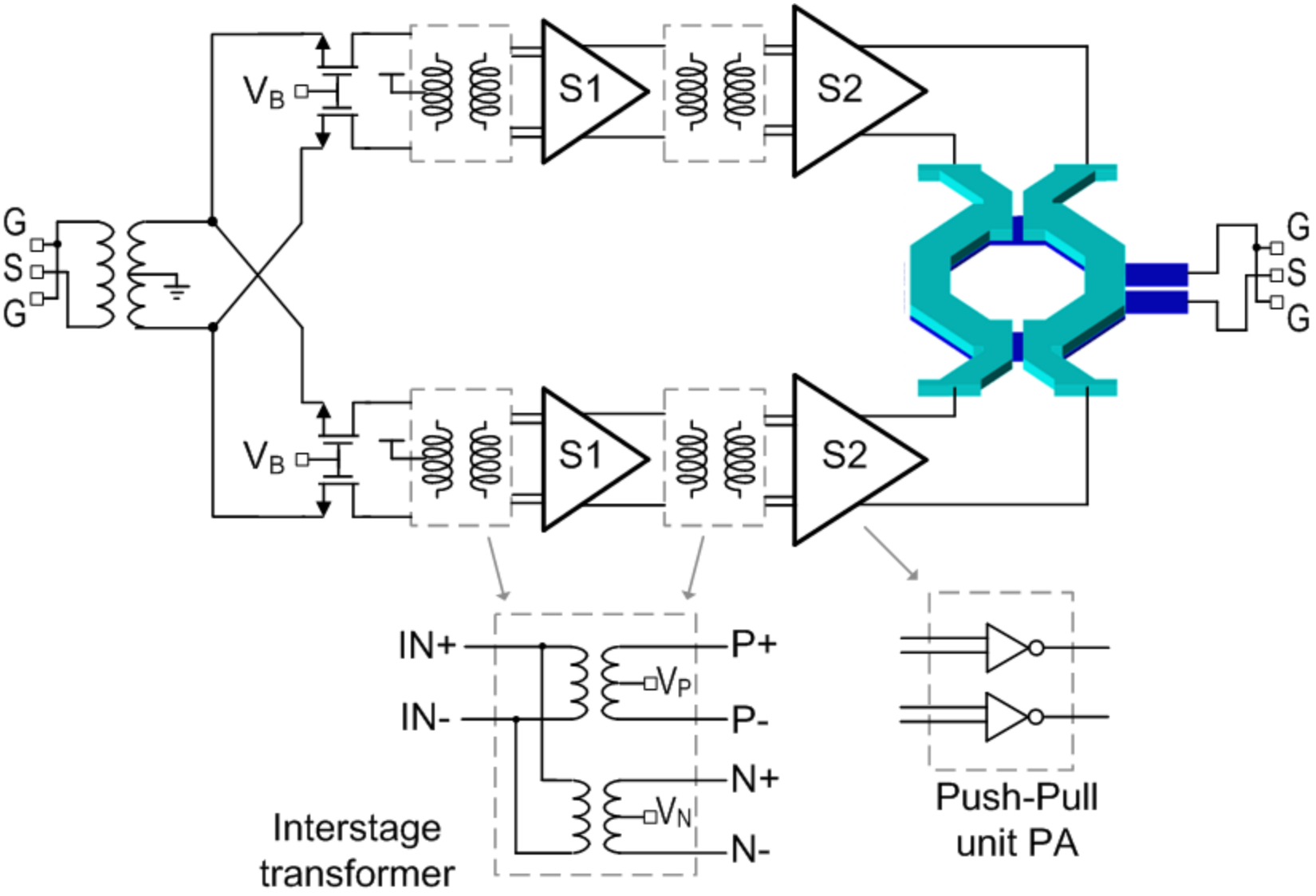
Push-Pull unit PA

- Complementary
  - PMOS 30% larger
- Neutralization
  - C_P
  - C_N
- Transformer
  - Two secondary
  - Individual bias
  - Optimization with width and overlap



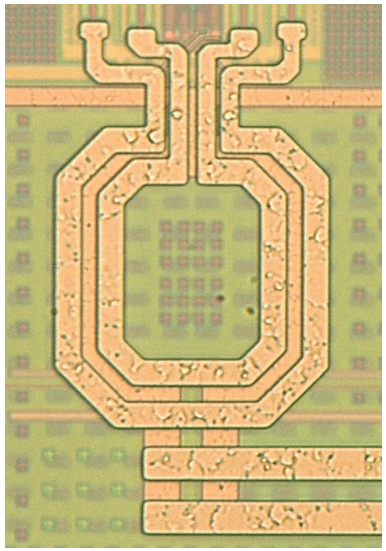


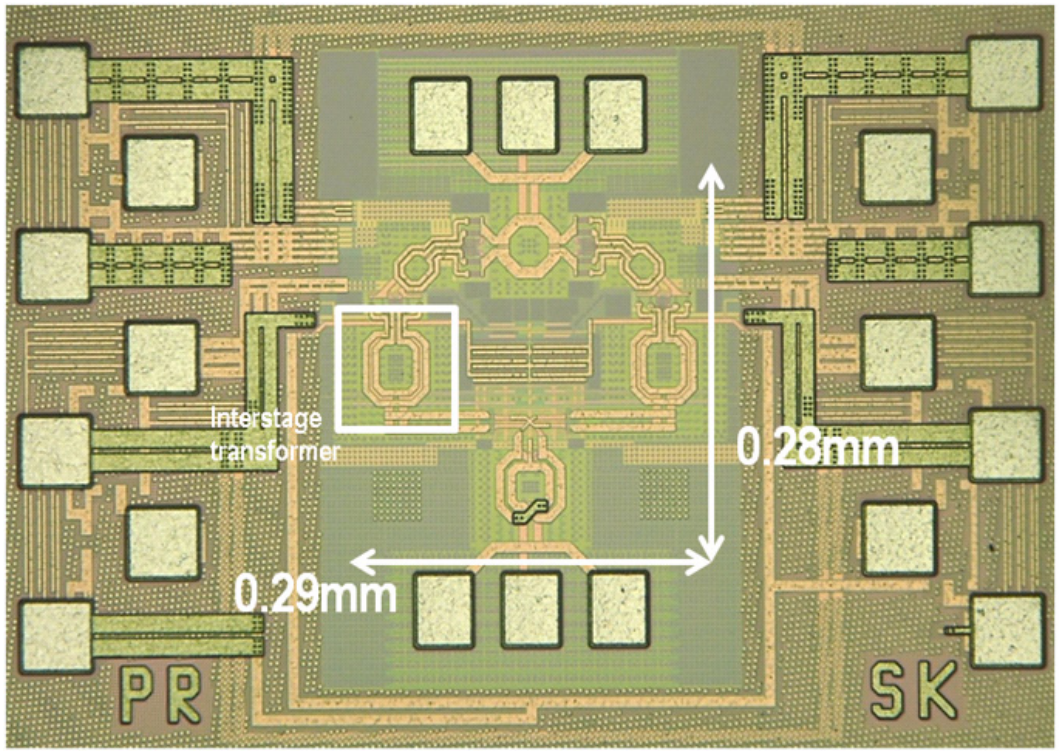
Architecture



Die photo

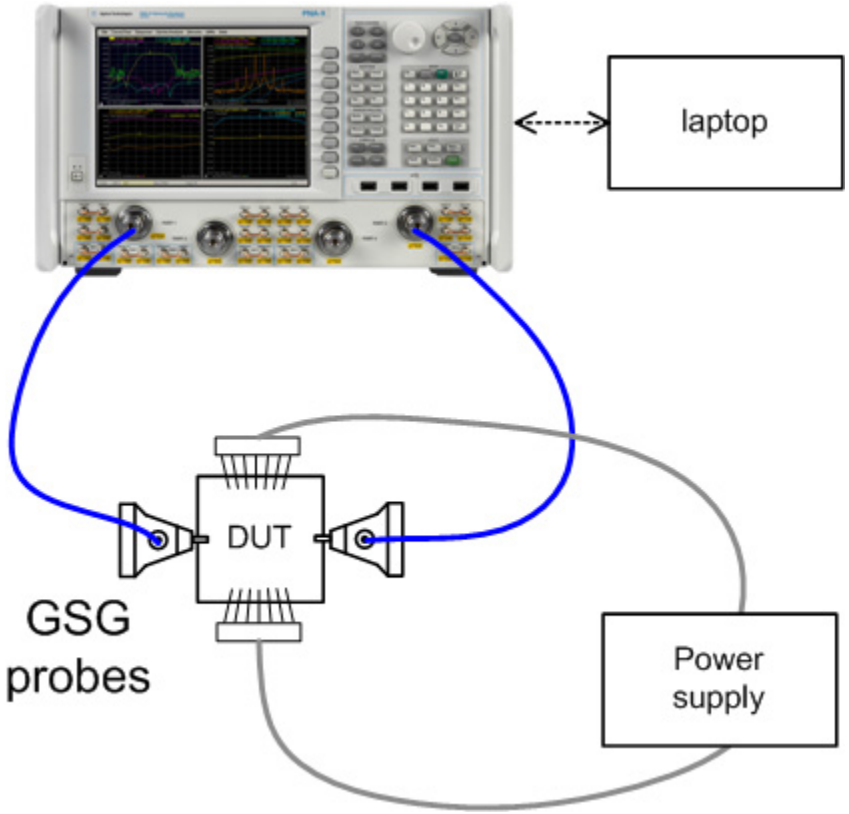
- 40nm GP CMOS
- Active area
  - < 0.09 mm^2





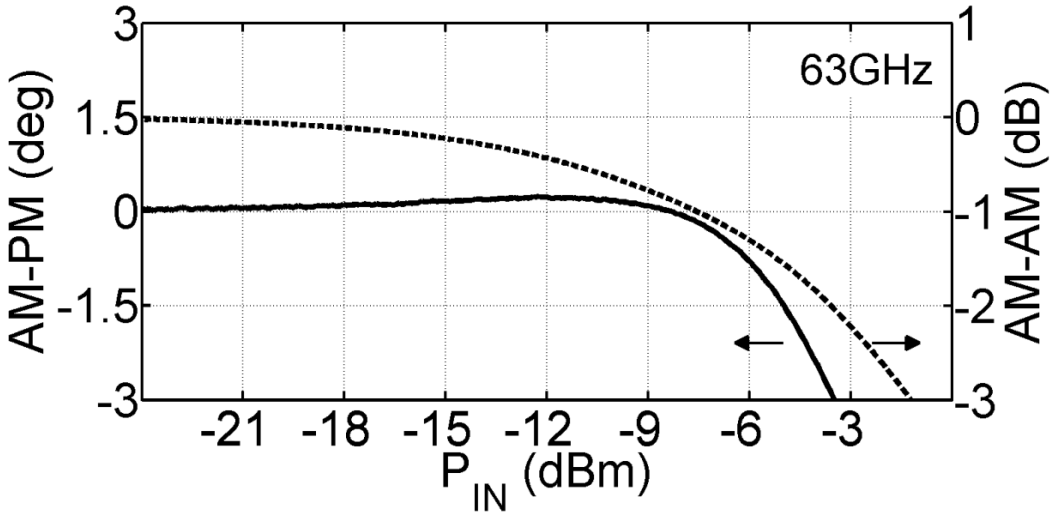
Measurement setup – AM-PM

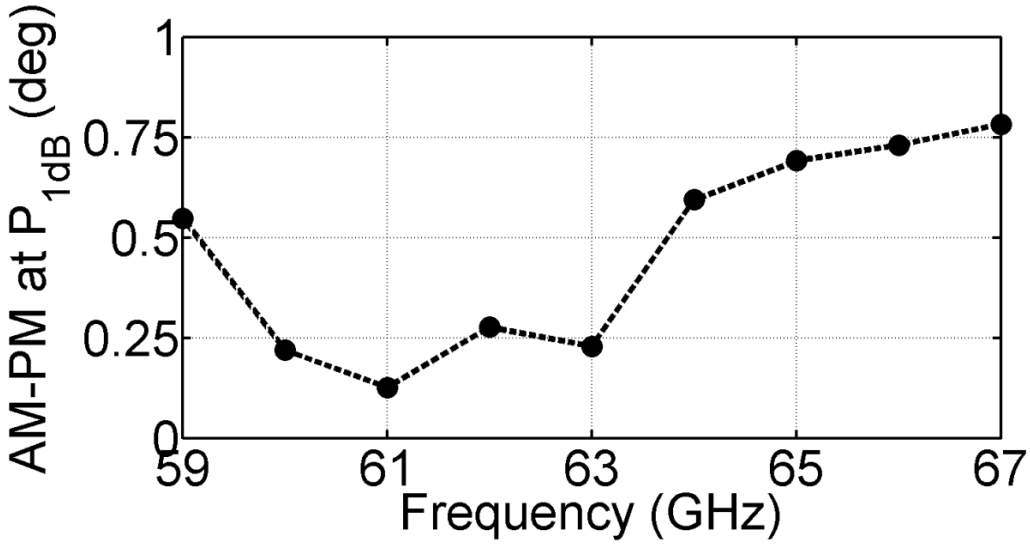
- PNA-X
  - 67 GHz Network analyzer
  - SOLT calibration
- swept power S-parameter measurement
  - AM-PM



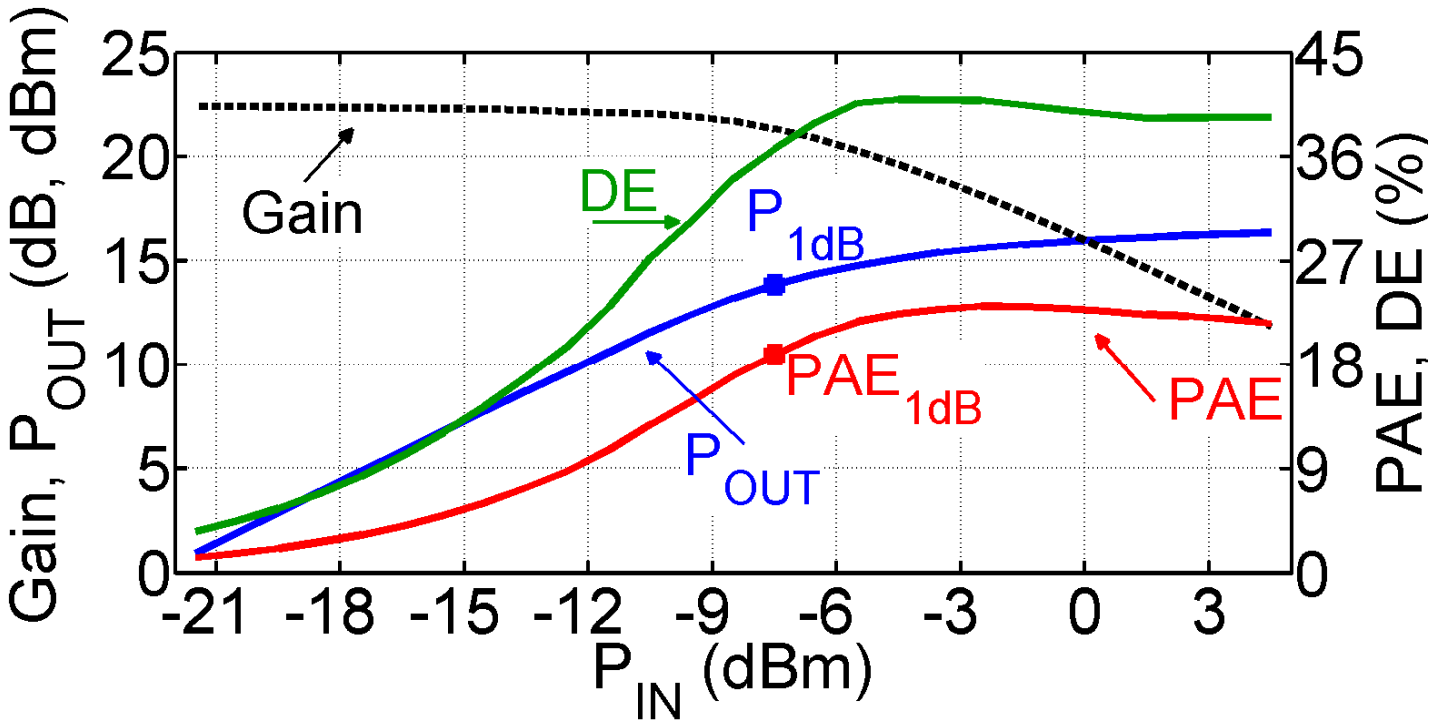
Measurements – AM-PM

- Cancellation of AM-PM distortion
  - Wideband
  - < 0.8°



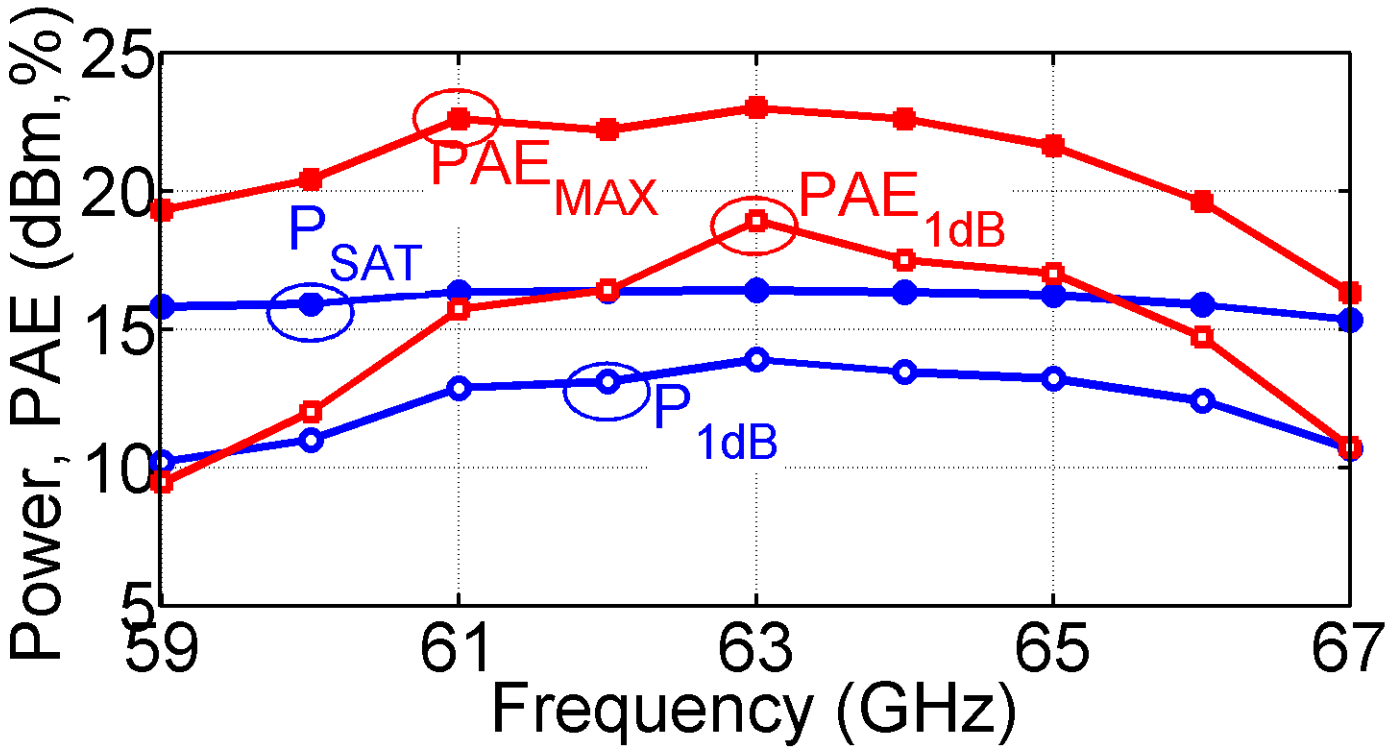


Measurements – CW



Gain	P_{SAT}	DE_{MAX}	PAE_{MAX}	PAE_{P1dB}
22.4dB	16.4dBm	40.9%	23.0%	18.9%

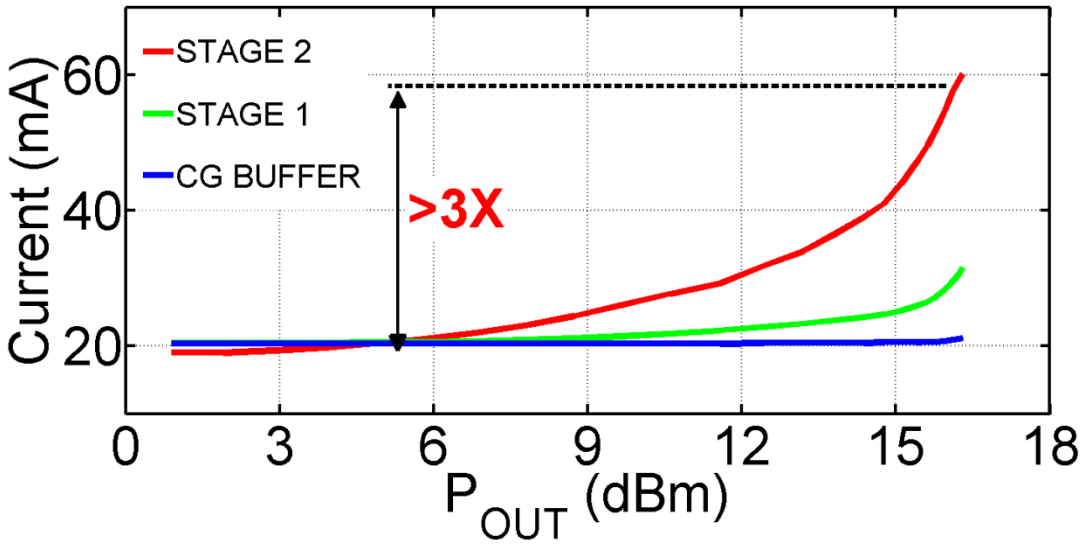
Measurements – CW vs freq

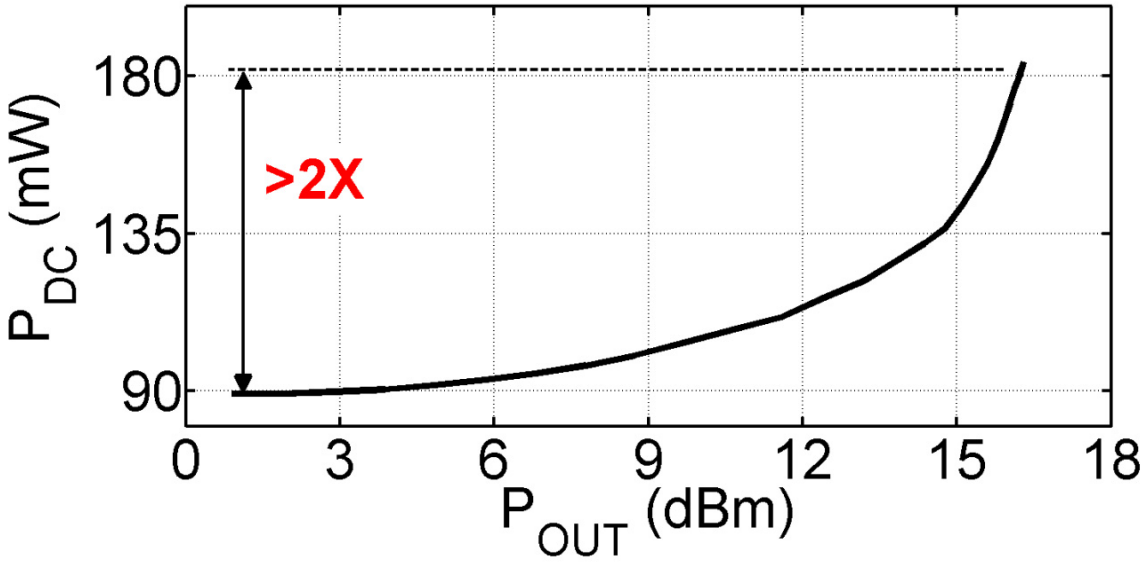


P_{SAT}	PAE_{MAX}
> 15.0dBm	>16.0%

Measurements – DC power

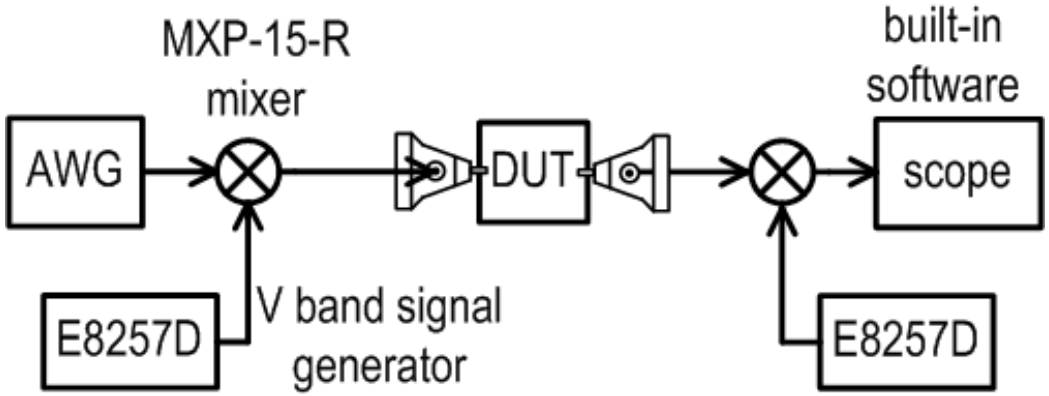
- DC current
  - Deep class AB mode for output stage
- DC power
  - more than halves from saturated



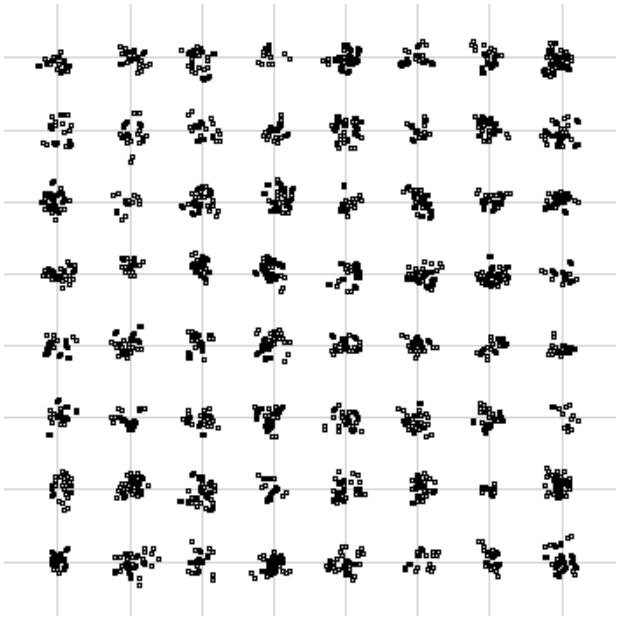


Measurements – QAM-64

- Modulation signal measurements



Signal	QAM-64
PAPR	8.1dB
Data-rate	3Gb/s
P_{AVG}	7dBm
EVM	-25.2dB



Comparison with 60GHz TX and PA

	This work	Zhao JSSC'12	Vidojkovic ISSCC'13	Okada JSSC'11	Siligaris ISSCC'11	Chen ISSCC'11	Zhao JSSC'13
Tech (nm)	**40**	40	40	65	65	65	40
Gain (dB)	**22.4**	26	22.5	18.3	16.4	20.3	17
P_{SAT} (dBm)	**16.4**	15.6	10	10.9	13	18.6	17
P_{1dB}(dBm)	**13.9**	15.6	8	9.5	8	15	13.8
PAE_{MAX}(%)	**23**	25	22.5	8.8	8	15.1	30.3
PAE_{1dB}(%)	**18.9**	25	16	<8.8	<8	6.8	21.6
PAE_{1db-5}(%)	**8**	10	7.4	2.5	NA	2	8.4
AM-PM (deg)	**0.2°**	15°†	-	-	-	-	0.2° AB / > 3° deep AB
modulated signal	**QAM-64**	QAM-16	QAM-16	QAM-16	OFDM QAM16	-	-

† φ-PM for 98% signal is <7°

Conclusion

- Demonstrated PMOS usage at mm-wave frequencies
- Using the proposed technique the AM-PM distortion has been minimized
- This enabled linear amplification of complex, high PAPR signals
- Without compromising the energy efficiency

A Class F^{-1}/F 24-to-31GHz Power Amplifier with 40.7% Peak PAE, 15dBm OP_{1dB}, and 50mW P_{sat} in 0.13μm SiGe BiCMOS

Seyed Yahya Mortazavi

Kwang-Jin Koh

Multifunctional Integrated Circuits & Systems Group

Virginia Tech, Blacksburg, VA

VirginiaTech
Invent the Future®

Outline

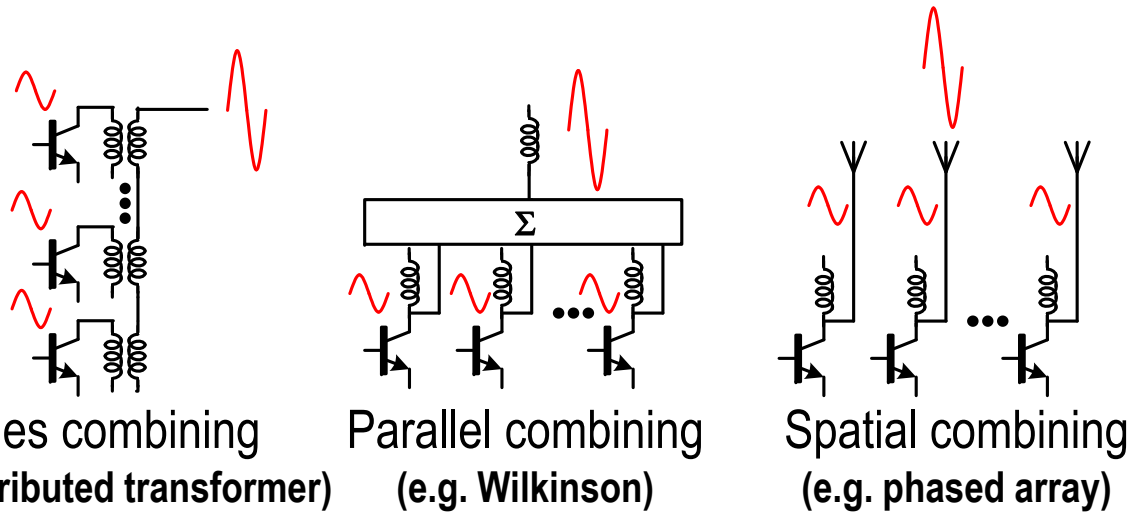
- Background / Motivation
  - Challenge in Silicon mm-Wave PAs
  - Efficiency of mm-Wave PAs
  - Harmonic Tuned (Class-F^{-1}, Class-F) PAs
- Class-F^{-1} to Class-F Mode-Transition PA Design
- Measurement Results
- Conclusion

Challenge in Silicon mm-Wave PAs

- Speed-breakdown tradeoff
- Not sufficient silicon transistor speed (f_T, f_{max}) for mm-wave

⇨ **Small P_{out} per PA stage**

- Power combining with a PA-array can increase P_{out}.

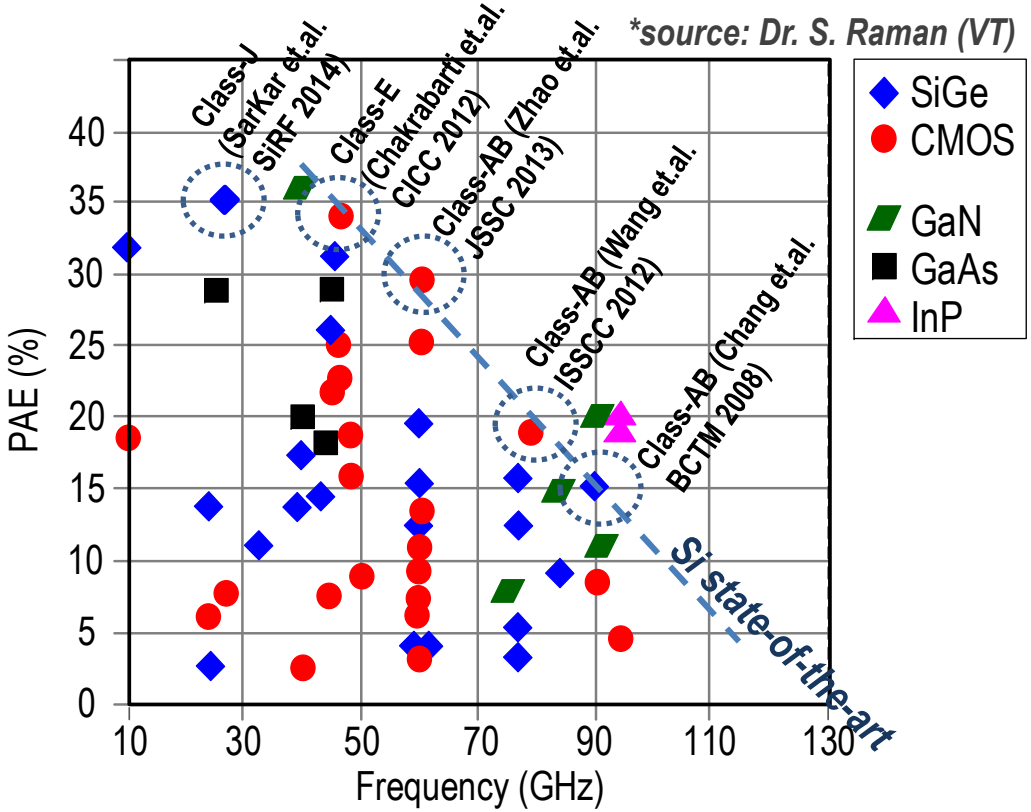


Series combining (e.g. distributed transformer) | Parallel combining (e.g. Wilkinson) | Spatial combining (e.g. phased array)

⇨ **Low power-added efficiency (PAE)**

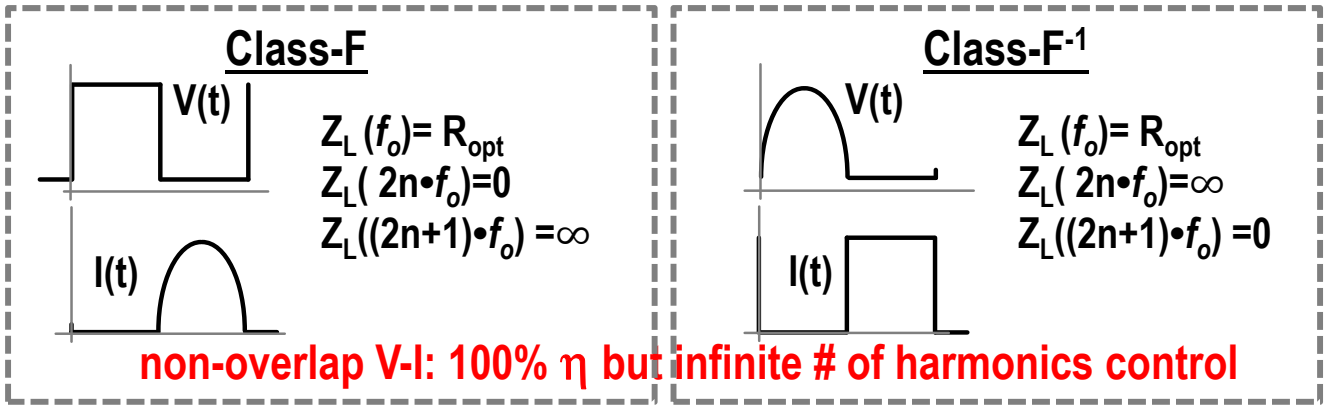
- It is critical to improve unit PA's PAE to improve overall PAE in a PA-array.
- Relatively, a lack of research on efficient PA topology suitable for mm-wave.

Efficiency of mm-Wave PAs



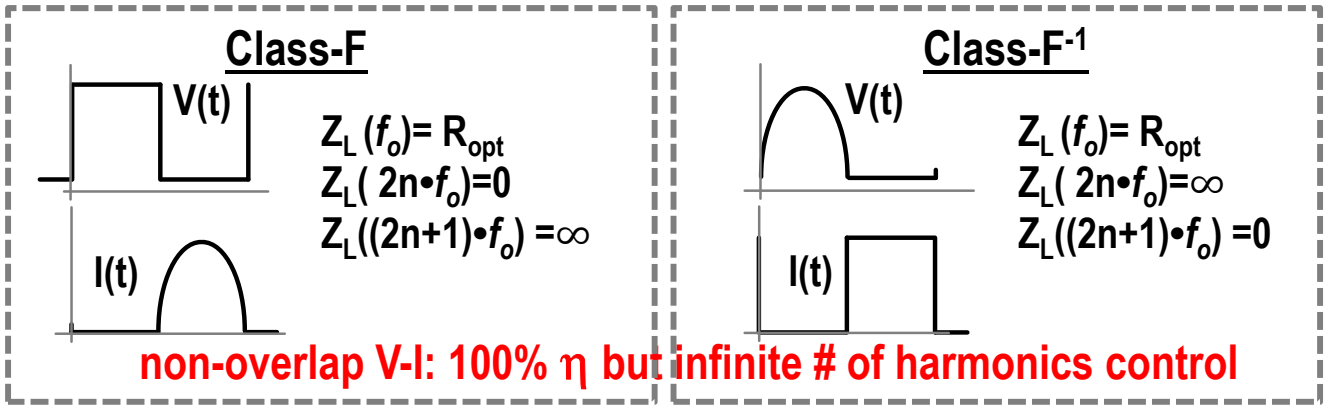
- With *Class-AB* , ~30% PAE has been reported at 60 GHz in 40 nm CMOS.
- *Class-E* PA has achieved ~30-35% PAE at ~45 GHz in 45 nm SOI CMOS.
- *While potentially viable technology, harmonic-tuned approaches (Class-F, Class-F^{-1}) has not been explored yet at mm-wave.*

Harmonic Tuned (Class-F, Class-F^{-1}) PAs



- In practice, ~ up to the 3rd harmonic power control at mm-wave with a finite V_{knee} (e.g. practical max. η ~90%x(V_{CC}-V_{knee})/V_{CC} =68% if V_{CC}=2V & V_{knee}=0.5V).

Harmonic Tuned (Class-F, Class-F^{-1}) PAs

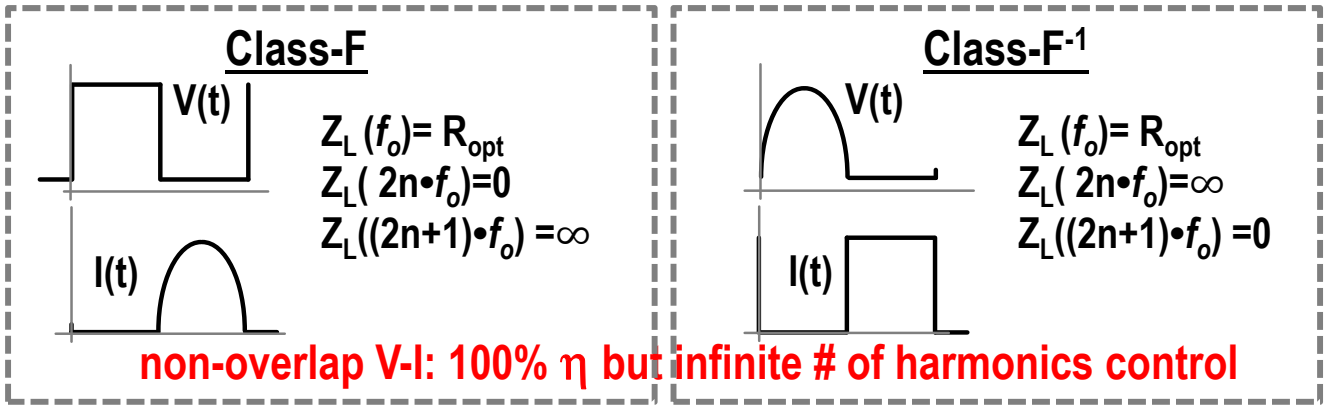


- In practice, ~ up to the 3rd harmonic power control at mm-wave with a finite V_{knee} (e.g. practical max. η ~90%x(V_{CC}-V_{knee})/V_{CC} =68% if V_{CC}=2V & V_{knee}=0.5V).

Pros:

- Current-mode: power transistor operates as a current source
- Class-AB biasing: fast speed, high gain
- No switching loss involved
- On-chip high-Q L-C networks are readily available for harmonic-Z control @mm-wave

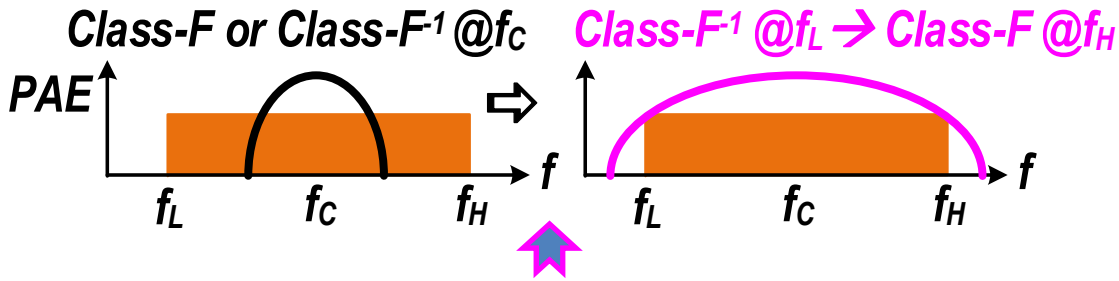
Harmonic Tuned (Class-F, Class-F^{-1}) PAs



- In practice, ~ up to the 3rd harmonic power control at mm-wave with a finite V_{knee} (e.g. practical max. η ~90%x(V_{CC}-V_{knee})/V_{CC} =68% if V_{CC}=2V & V_{knee}=0.5V).

Pros:

- Current-mode: power transistor operates as a current source
- Class-AB biasing: fast speed, high gain
- No switching loss involved
- On-chip high-Q L-C networks are readily available for harmonic-Z control @mm-wave

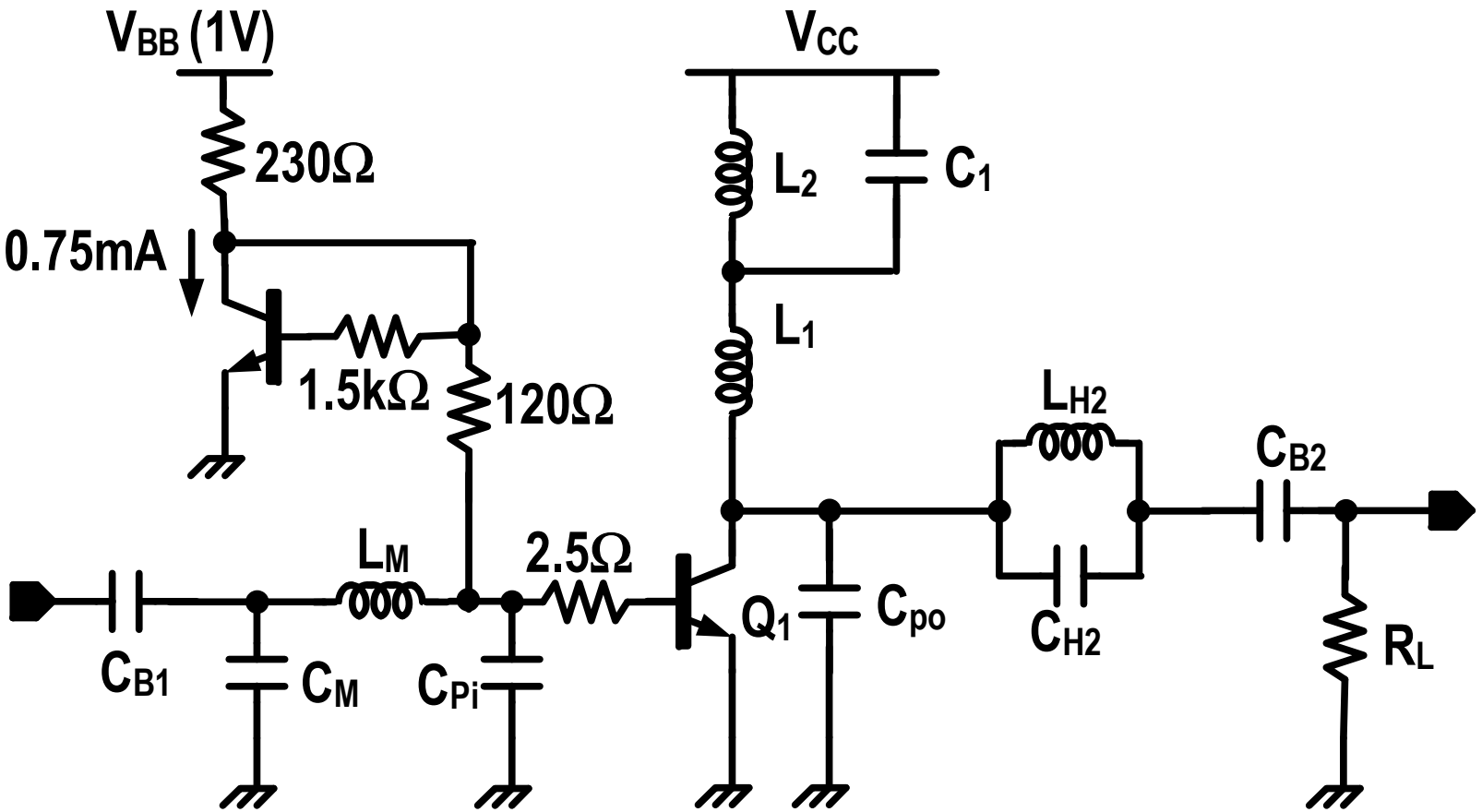


Cons:

- Narrowband PAE

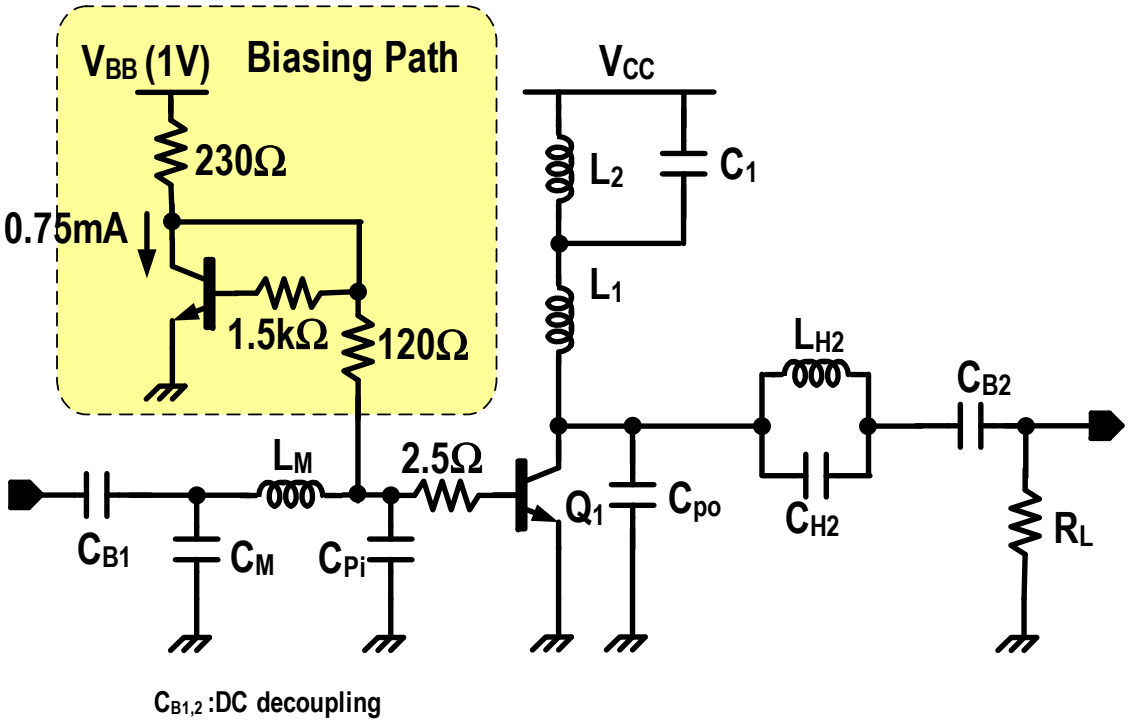
⇨ Need a wideband technique: motivation of *"mode-transition" operation.*

Proposed Class-F^{-1} to Class-F Mode-Transition PA



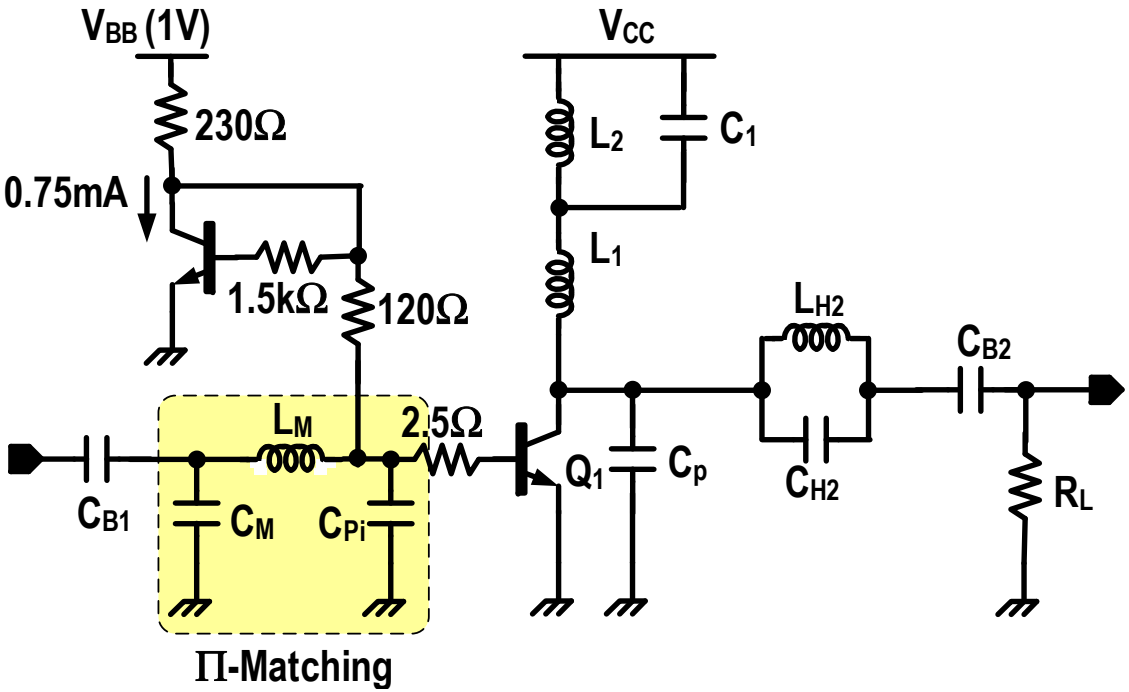
$C_{B1,2}$:DC decoupling

Class-F^{-1} to Class-F Mode-Transition PA (1)



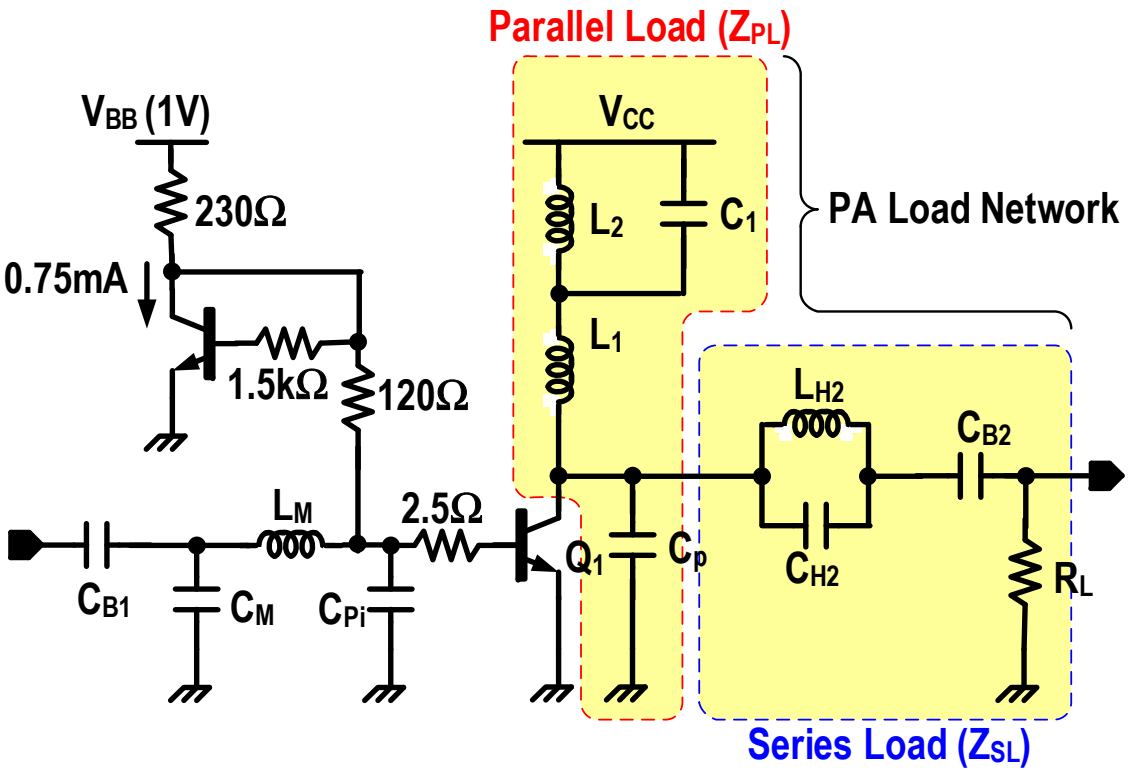
- Class-AB biasing: V_{BE}=0.85 V & I_{CE}=9 mA (V_{CC}=2.2 V, V_{knee}=0.5 V)
- Sizing for peak f_T (~180 GHz) @P_{sat}=50 mW
- Impedance seen from base is < 300-Ω so that $V_{CE,\,peak}$ ~ 3xBV_{CEO}~5 V @Class-F^{-1} (BV_{CEO}~1.7 V & BV_{CBO}~5.5 V)

Class-F^{-1} to Class-F Mode-Transition PA (2)



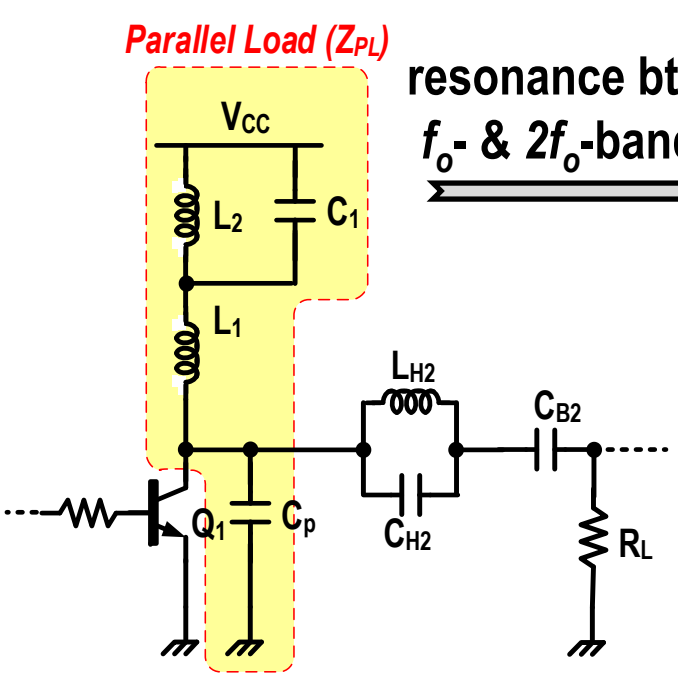
- Π-matching network provides a wideband Z-matching: S_{11} < -10 dB @23-31 GHz (sim.).
- C_{pi} includes base-node parasitic capacitances including layout parasitics.
- 2.5 Ω base resistance stabilizes the PA over all operation frequencies.

Class-F^{-1} to Class-F Mode-Transition PA (3)

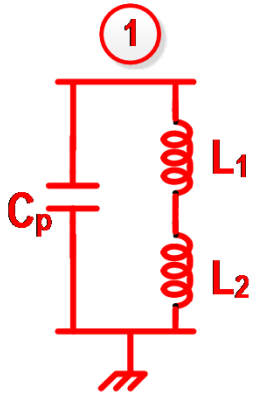


- Z_{PL} & Z_{SL} comprise multi-resonance harmonic tuned load, cooperatively shaping an optimum load impedance for Class-F^{-1} and Class-F operations.
- C_p includes collector-node parasitic capacitances including layout parasitics.
- *L2-C1 tank impedance variation over harmonic frequencies plays a key role in transferring from Class-F^{-1} to Class-F over 24-31 GHz (see next slides).*

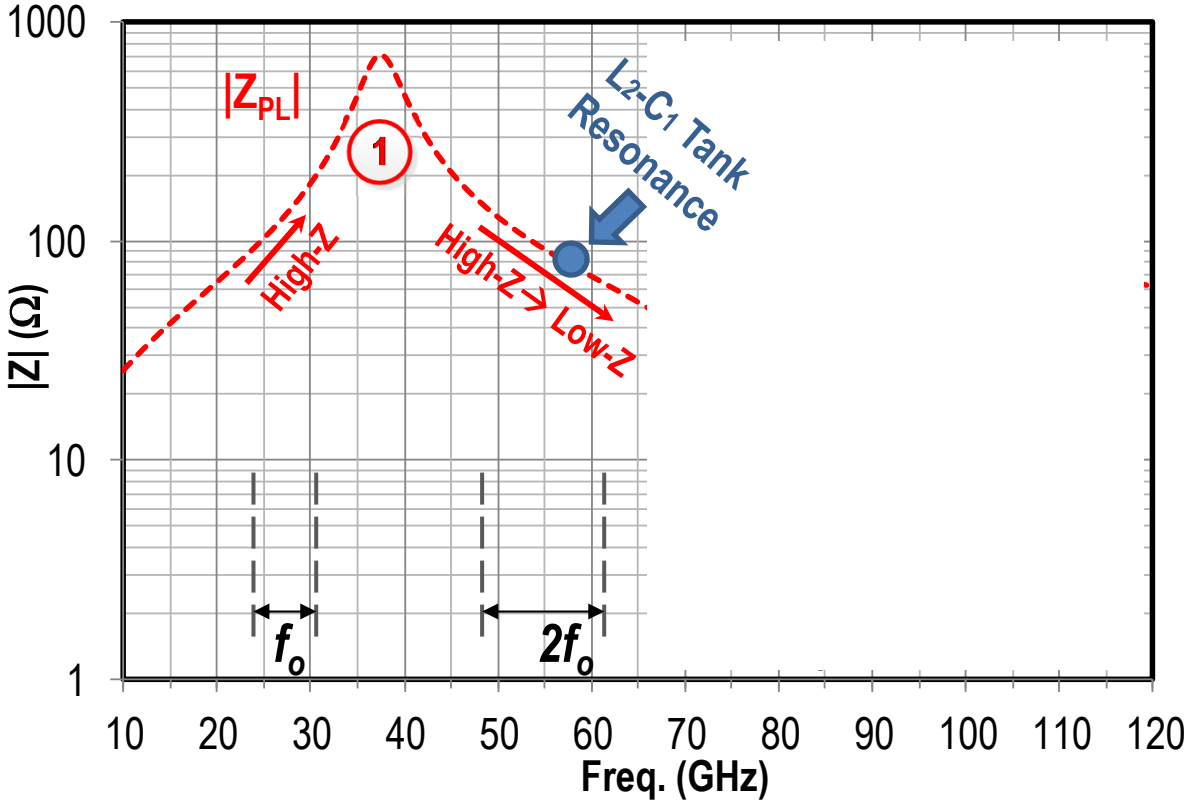
Load Network with F^{-1}/F Mode Transition (1)



resonance btw f_o- & $2f_o$-band



This tank provides relatively high impedance for both fundamental (f_o) and the 2nd harmonic ($2f_o$) bands.

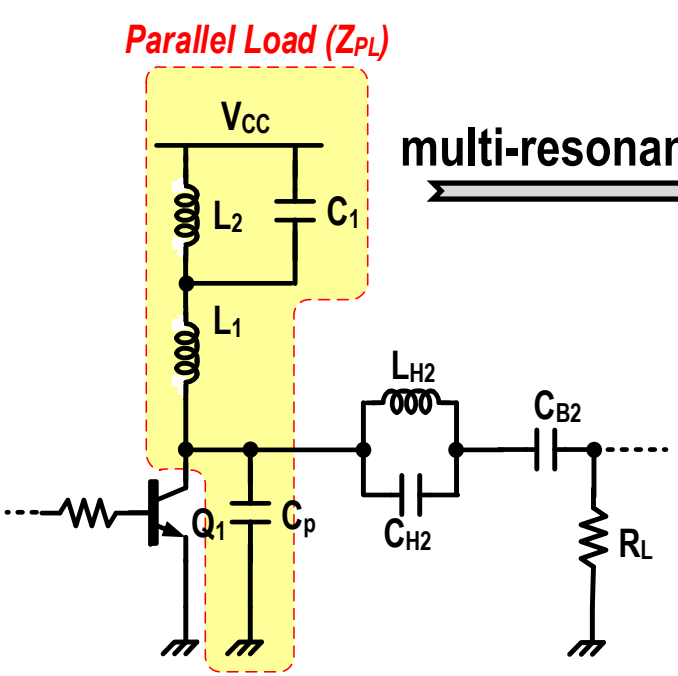


Z_{PL} Modulation by L_2-C_1 Tank

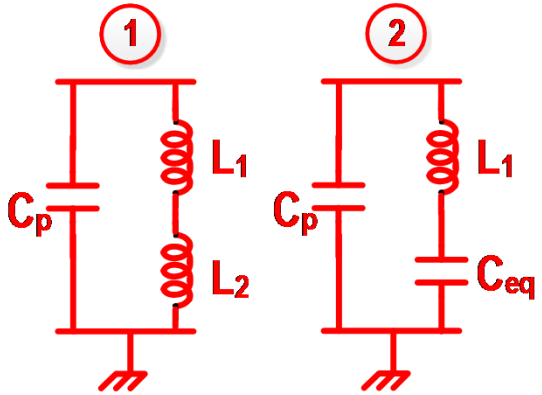
①: $L_2 \,||\, C_1 \sim L_2$

→ $Z_{PL} = s(L_1+L_2) \,||\, 1/sC_P$

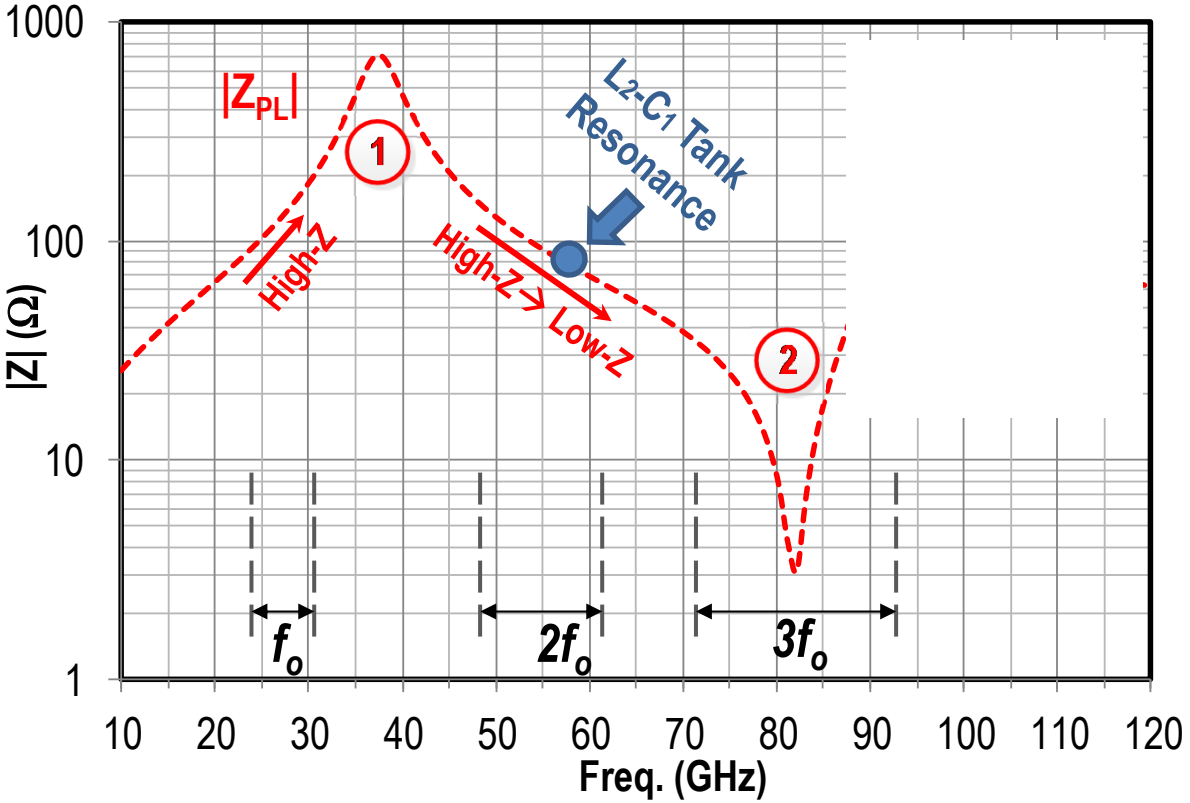
Load Network with F^{-1}/F Mode Transition (2)



multi-resonance



L_1-C_{eq} series resonance forms a sharp impedance null in the middle of the 3rd harmonic ($3f_o$) band .

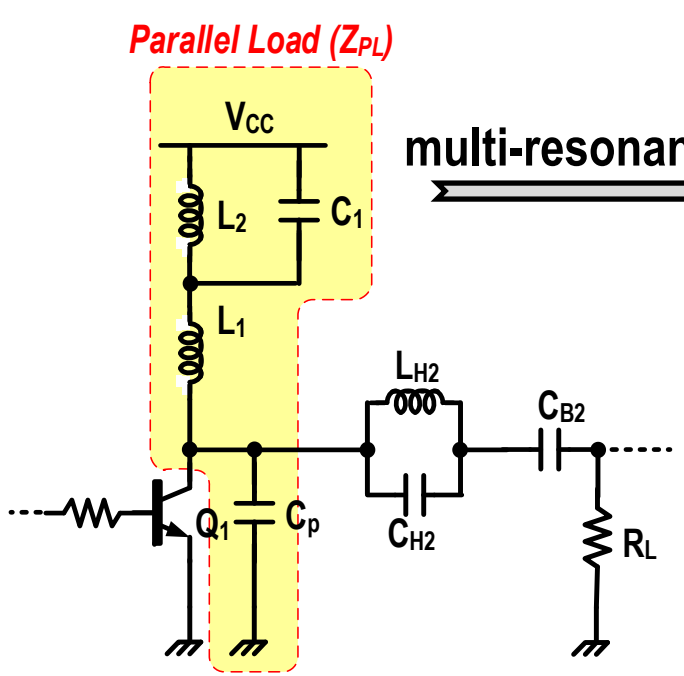


Z_{PL} Modulation by L_2-C_1 Tank

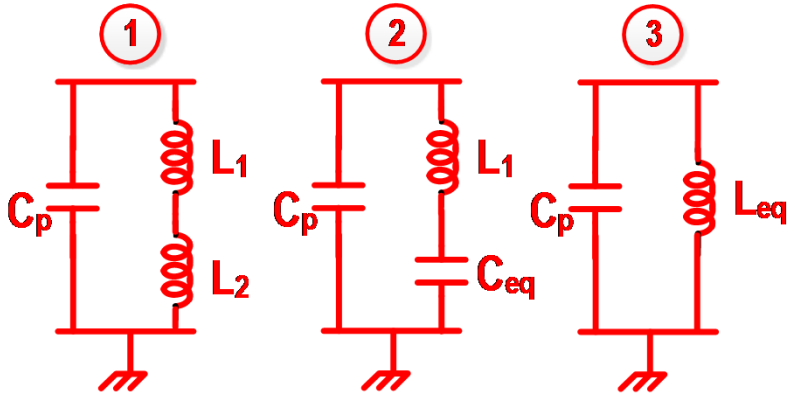
①: $L_2 \| C_1 \sim L_2$
→ $Z_{PL}=s(L_1+L_2) \| 1/sC_P$

②: $L_2 \| C_1 \sim C_{eq}$
→ $Z_{PL}=sL_1+1/sC_{eq}$

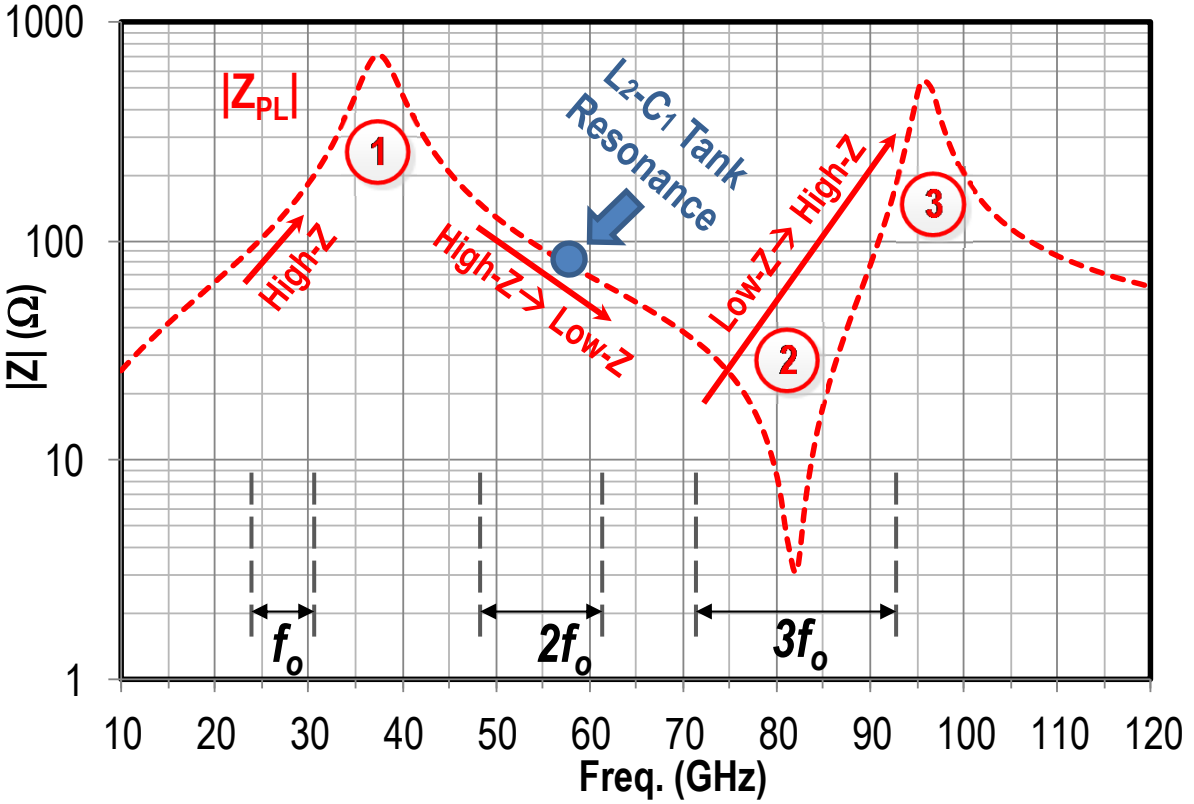
Load Network with F^{-1}/F Mode Transition (3)



multi-resonance



L_{eq}-C_P parallel resonance forms an impedance maxima at the edge of the $3f_o$-band.



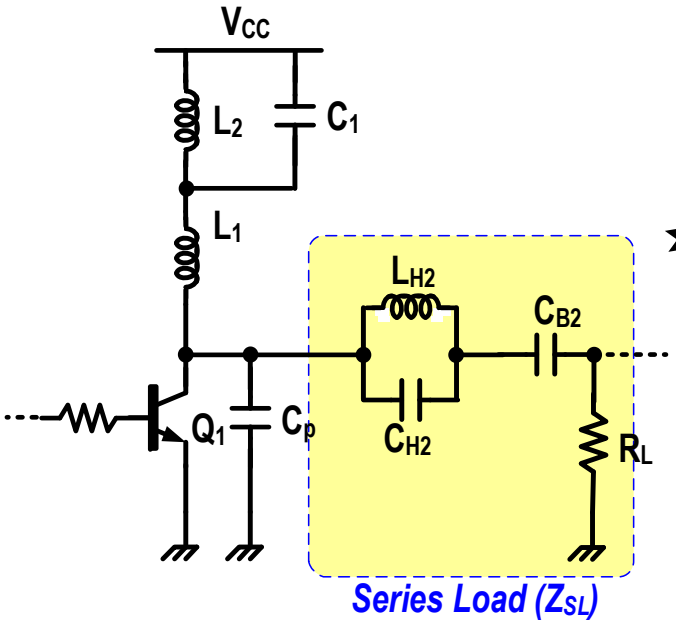
Z_{PL} Modulation by L_2-C_1 Tank

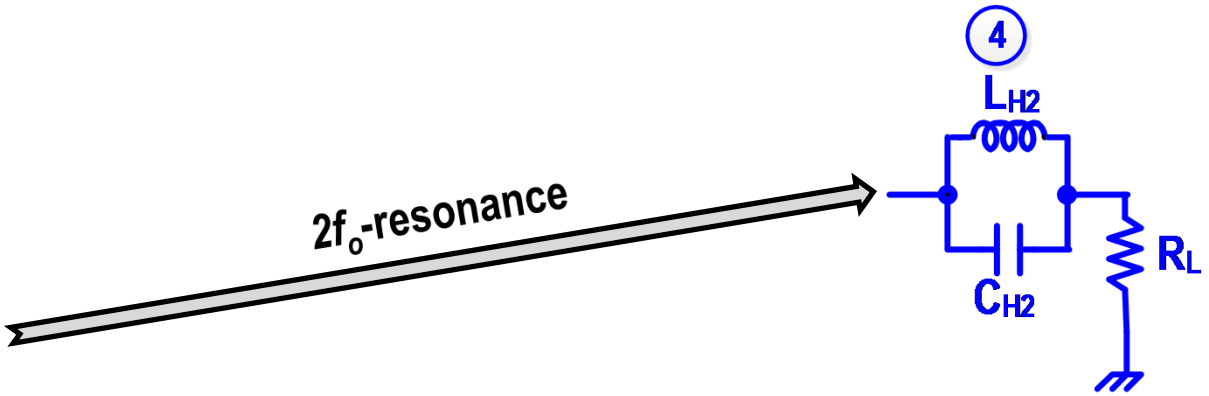
①: $L_2 \| C_1 \sim L_2$
→ $Z_{PL}=s(L_1+L_2) \| 1/sC_P$

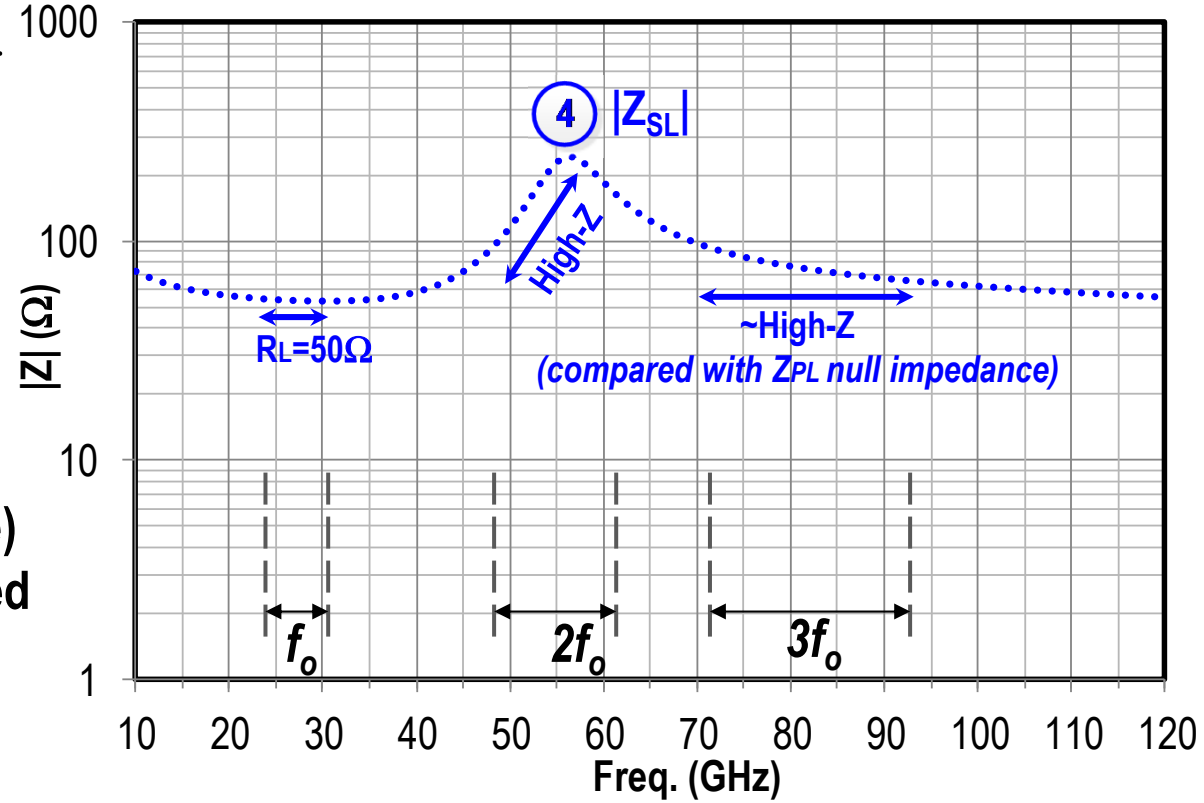
②: $L_2 \| C_1 \sim C_{eq}$
→ $Z_{PL}=sL_1+1/sC_{eq}$

③: L_1–$C_1 \sim L_{eq}$
→ $Z_{PL}=sL_{eq} \| 1/sC_P$

Load Network with F^{-1}/F Mode Transition (4)



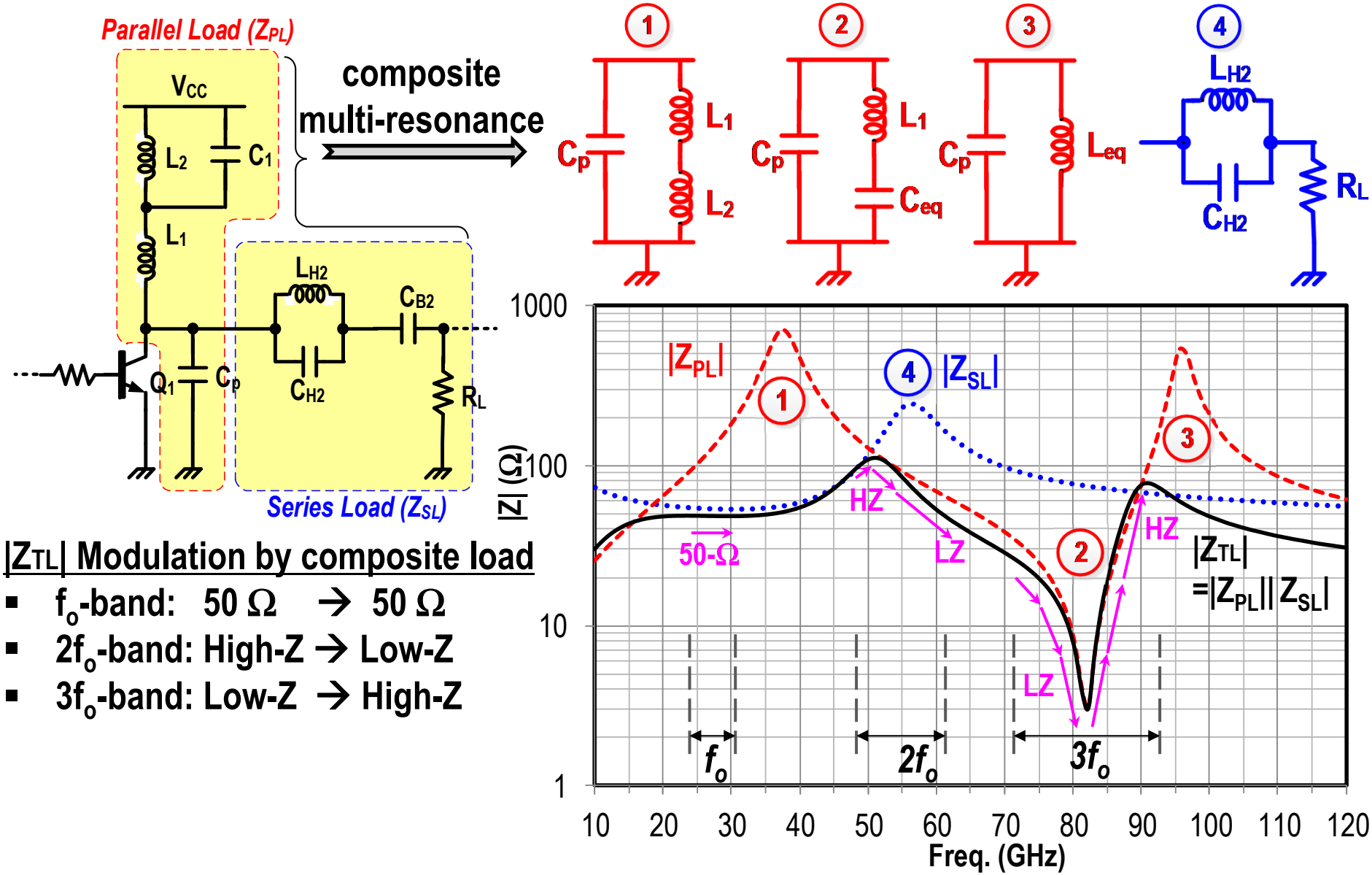




ZSL Modulation by LH2-CH2 Tank

- f_o-band: ~ constant 50 Ω
- $2f_o$-band: High-Z (resonance)
- $3f_o$-band: ~ High-Z (compared with ZPL null impedance)

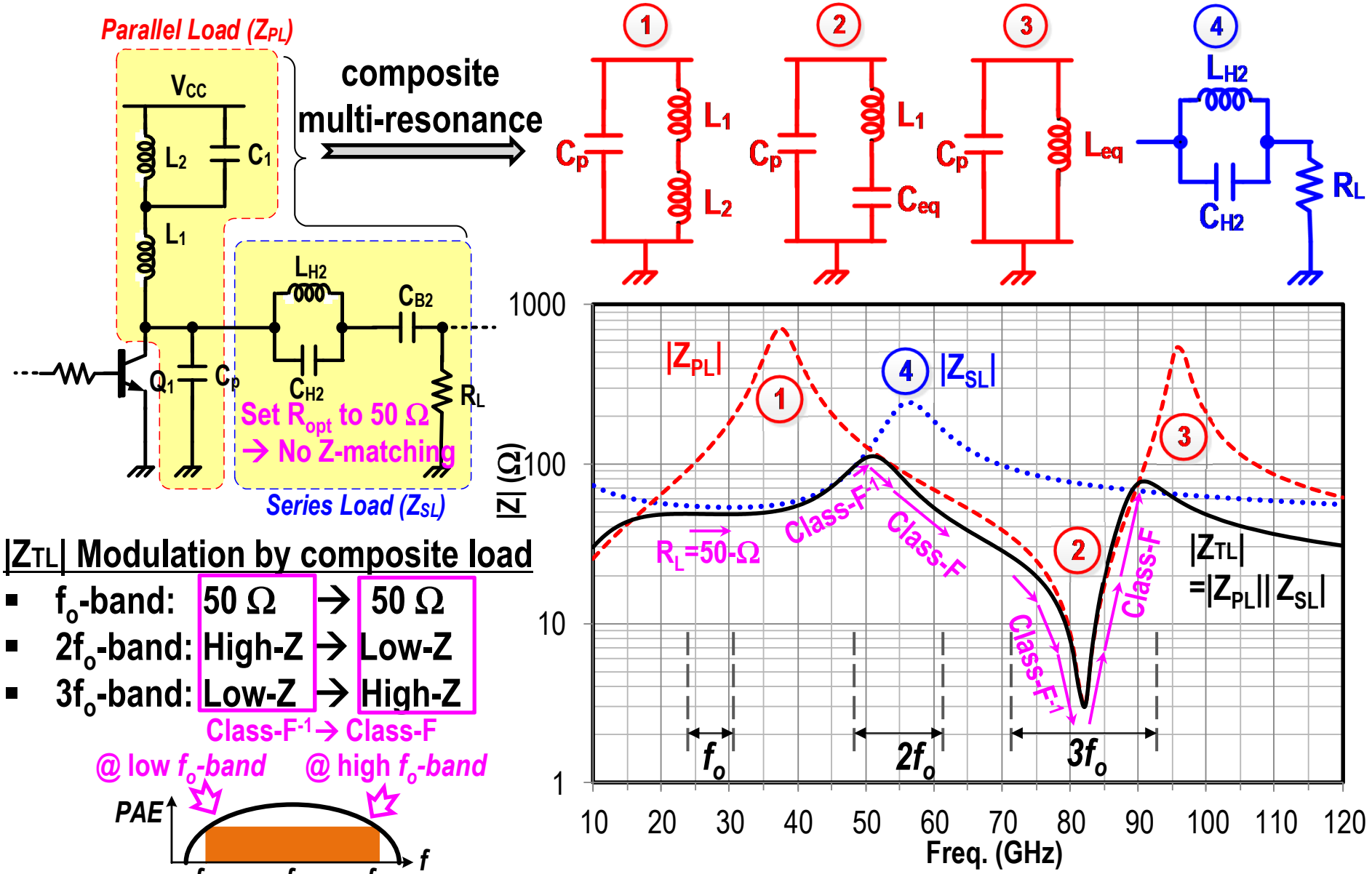
Load Network with F^{-1}/F Mode Transition (5)



$|Z_{TL}|$ Modulation by composite load

- f_o-band: 50 Ω → 50 Ω
- $2f_o$-band: High-Z → Low-Z
- $3f_o$-band: Low-Z → High-Z

Load Network with F^{-1}/F Mode Transition (6)



$|Z_{TL}|$ Modulation by composite load

- f_o-band: 50 Ω → 50 Ω
- $2f_o$-band: High-Z → Low-Z
- $3f_o$-band: Low-Z → High-Z

Class-F^{-1} → Class-F

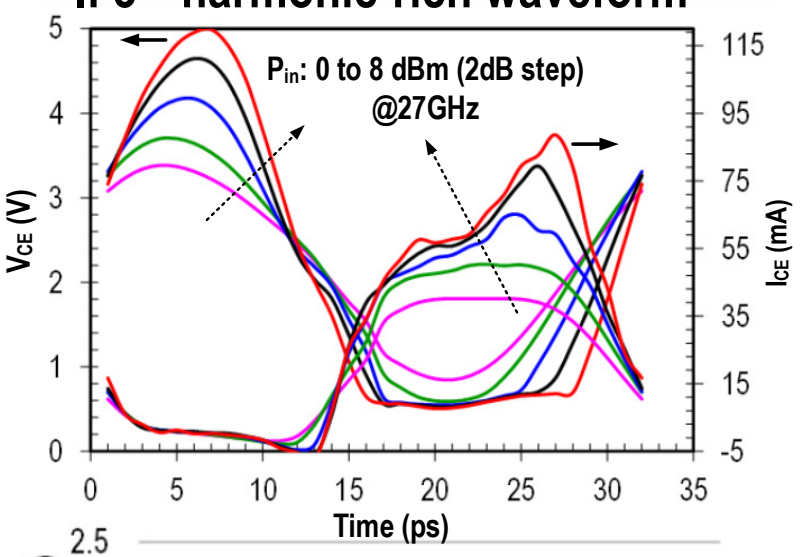
@ low f_o-band @ high f_o-band

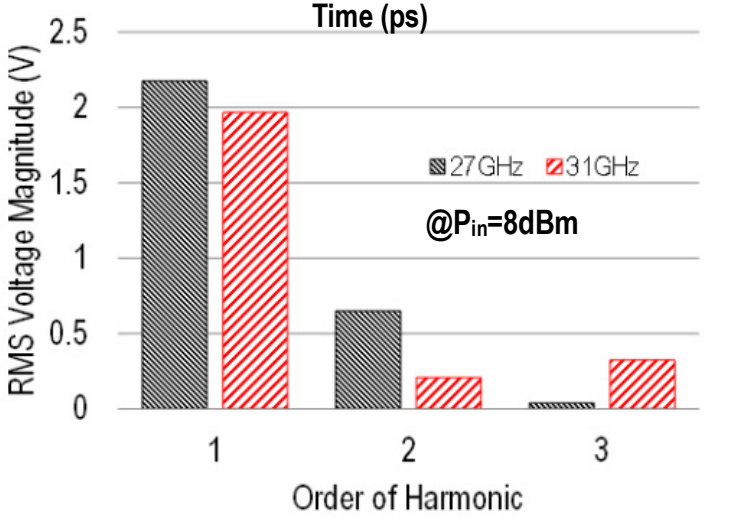
Simulated Collector V-I Waveforms (1)

Class-F^{-1} @27-GHz, P_{in}=8-dBm

V: Half-sinusoidal peaking

I: 3rd-harmonic-rich waveform

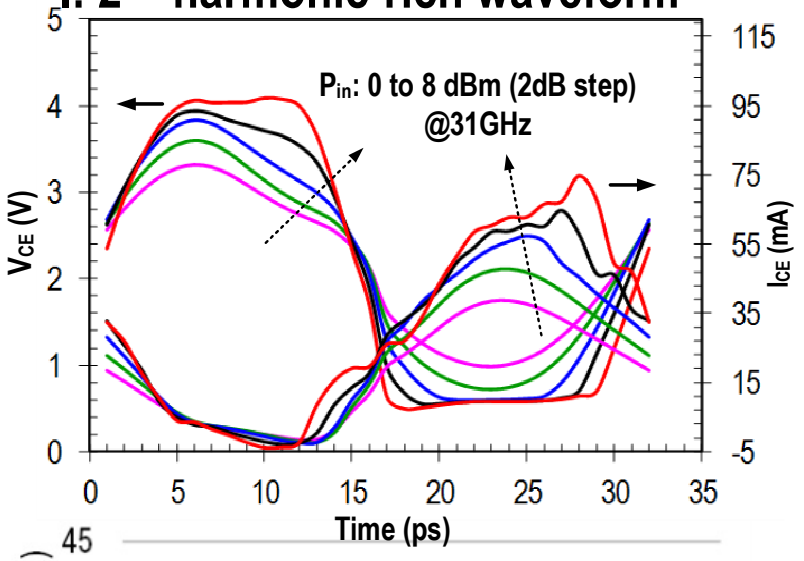


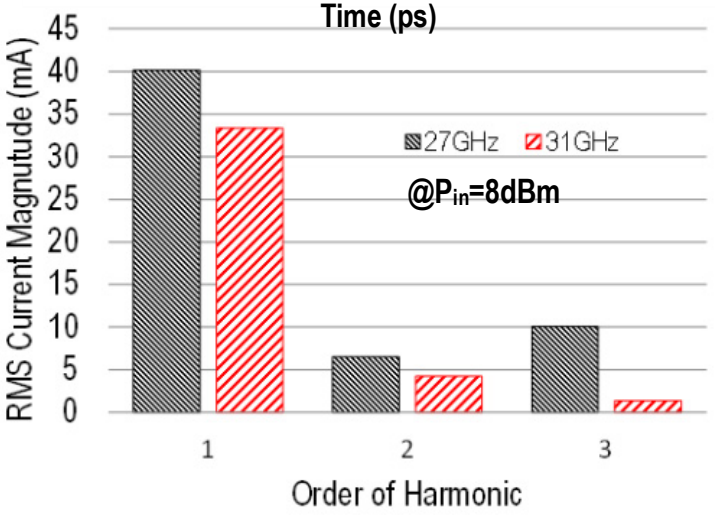


Class-F @31-GHz, P_{in}=8-dBm

V: Square-wave-like (3rd-harmonic rich)

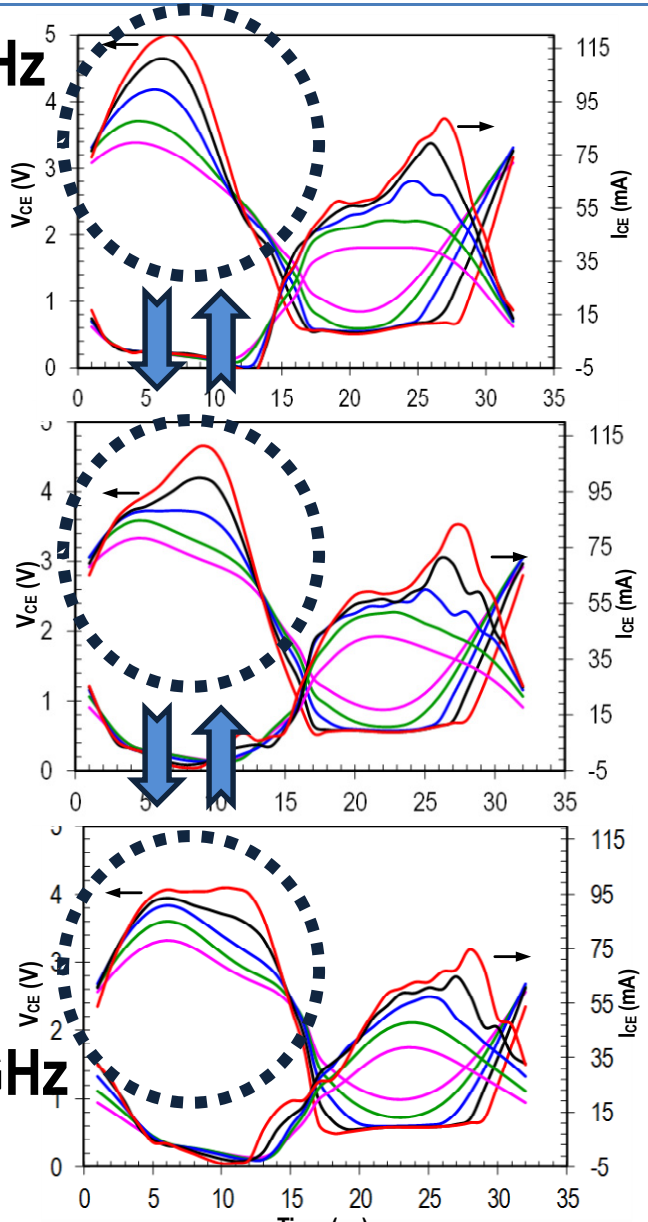
I: 2nd-harmonic-rich waveform





Simulated Collector V-I Waveforms (2)

Class-F^{-1} @27-GHz

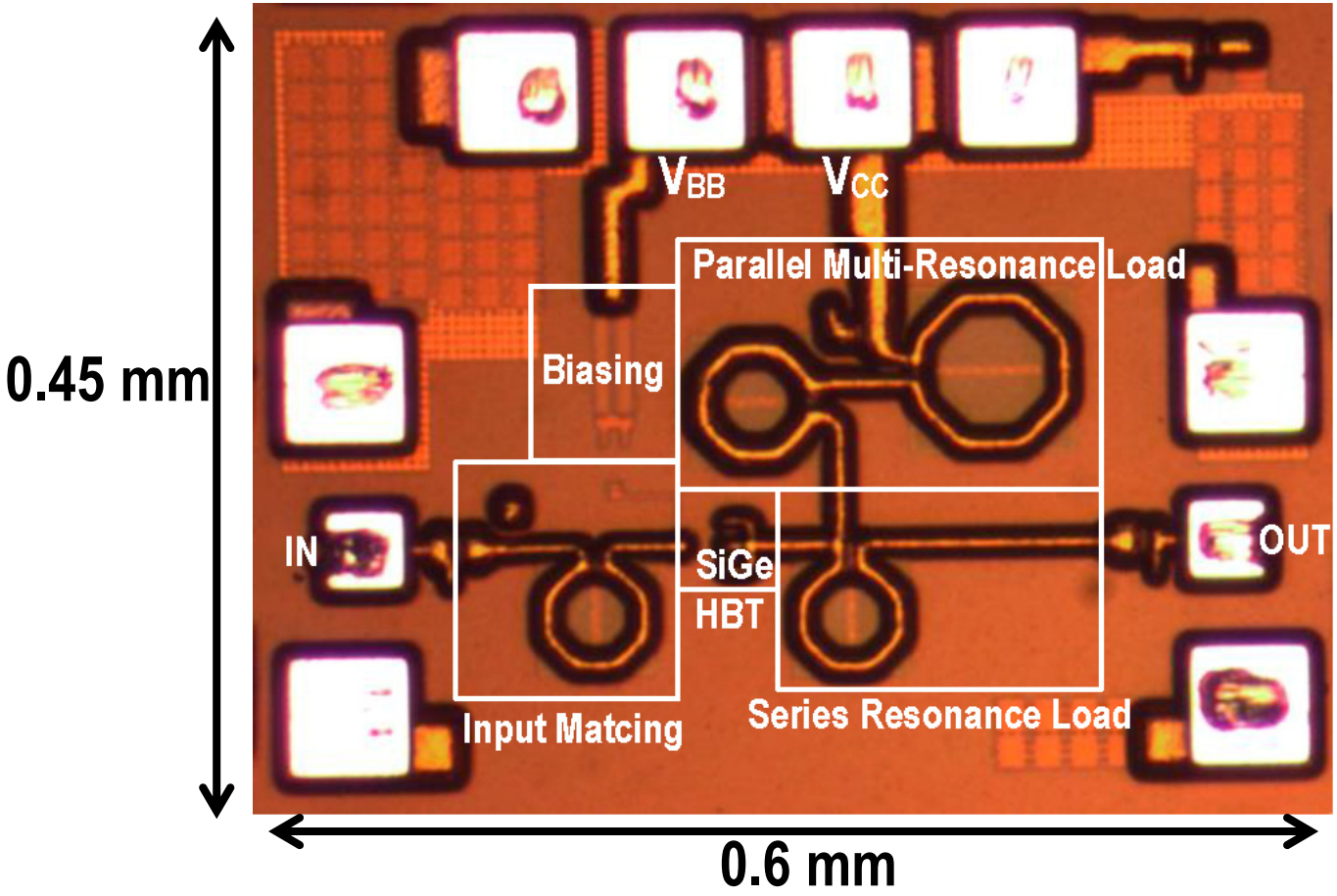


Transition mode @29-GHz

- Transitional ambivalent voltage waveforms between Class-F^{-1} & Class-F.
- Still can maintain a high-efficiency (similar to "*continuous Class-F*).

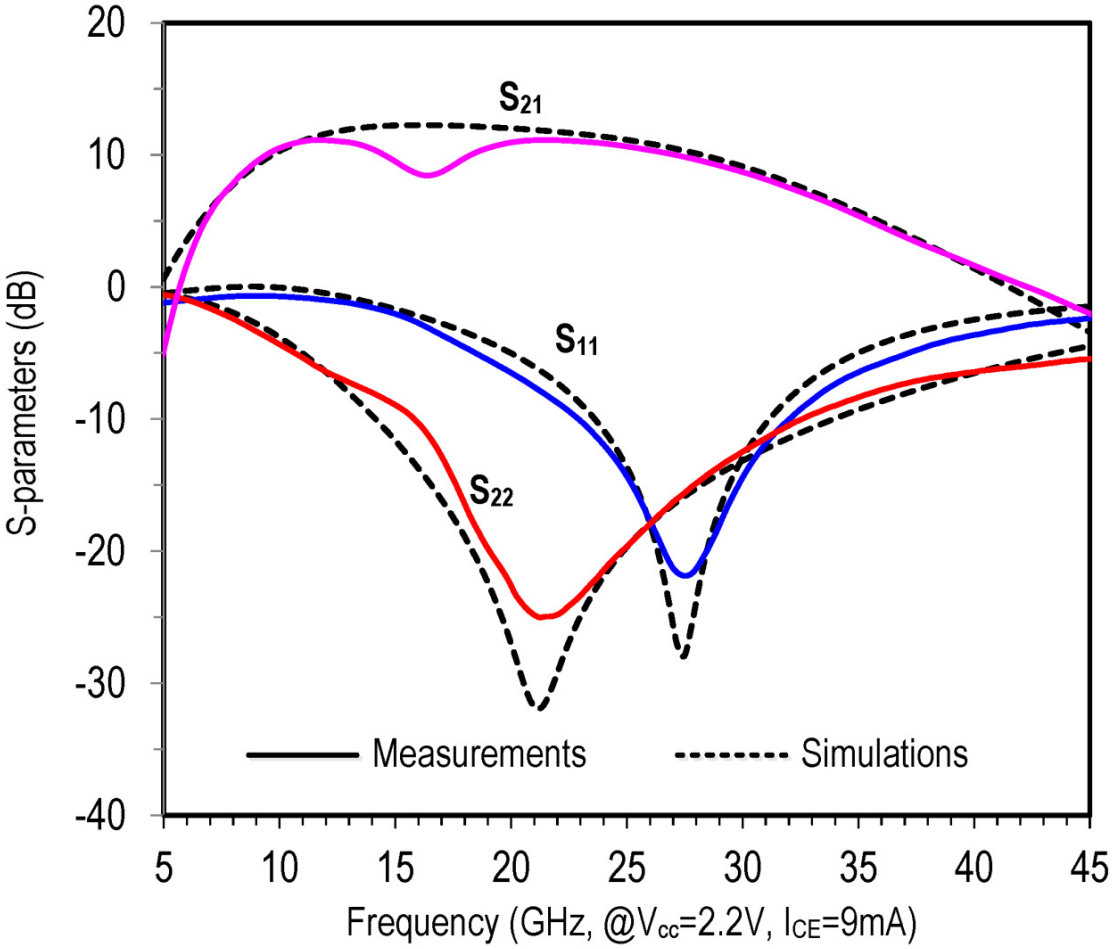
Class-F @31-GHz

Chip Photograph

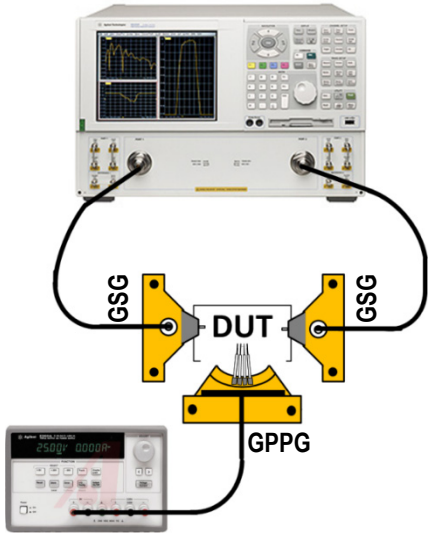


- IBM 8HP SiGe BiCMOS (f_T=180 GHz, f_{max}=200 GHz)
- Chip area: 0.6x0.45 mm^2 (w/i pads), 0.48x0.3 mm^2 (w/o pads)

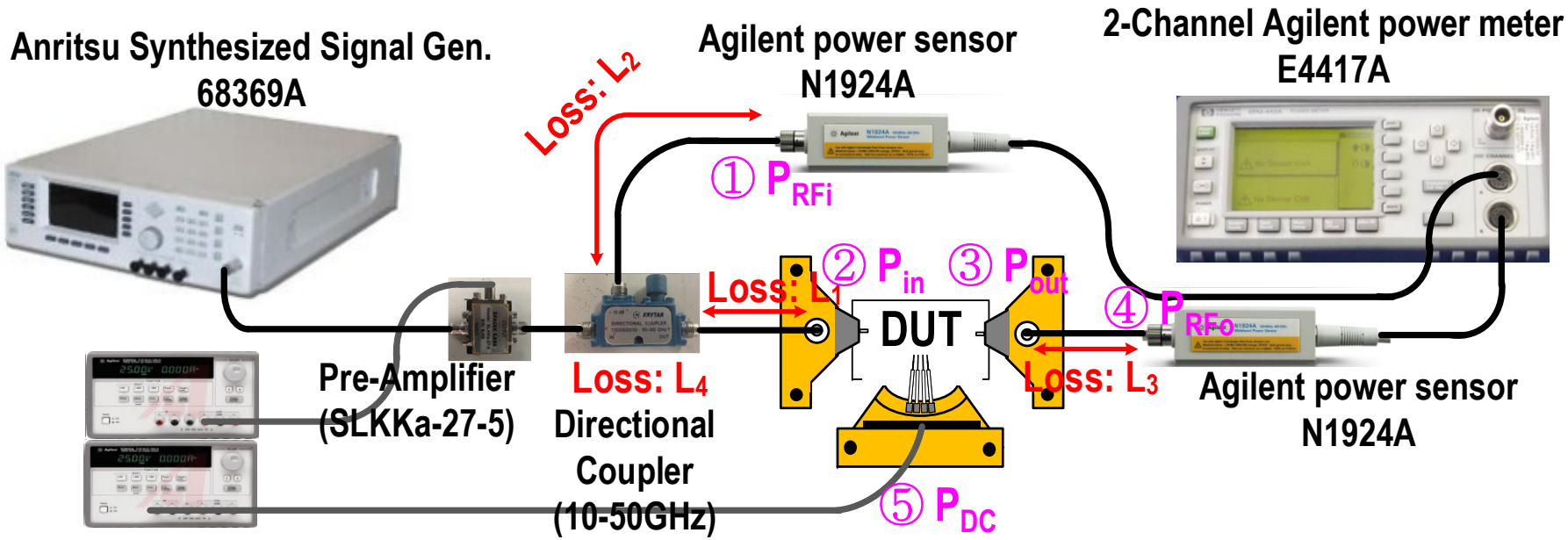
Small-Signal S-Parameters



- SOLT calibration
- Class-AB biasing (V_{CC}=2.2, I_{CE}=9mA)
- S_{21} = 9-10.8 dB : 24~31 GHz
- S_{11} < -10 dB : 22.5~32 GHz
- S_{22} < -10 dB : 15~33 GHz
- K-factor > 1



Large-Signal Measurement Setup

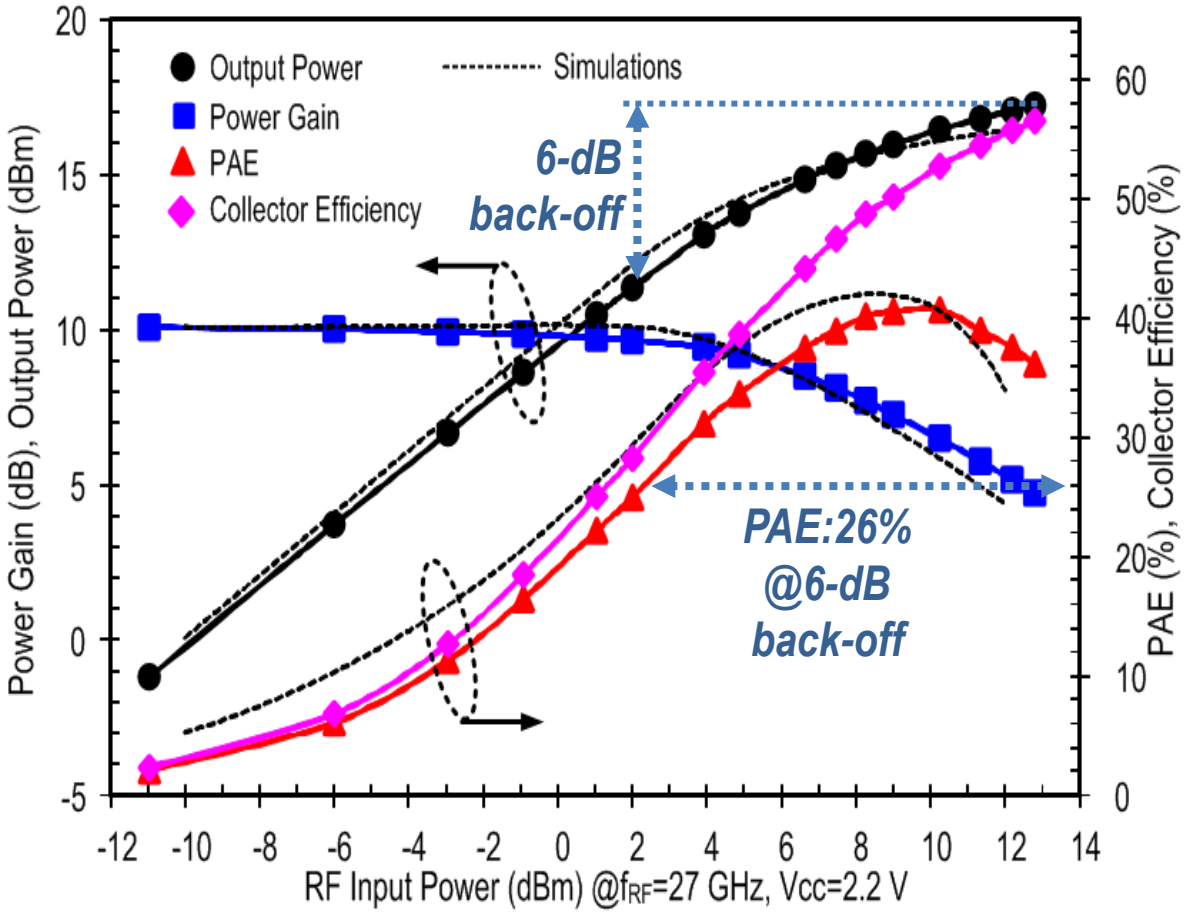


Power Calibration

- L_1, L_2 & L_3 : cable losses, L_4: coupler loss (typ. 10 dB @24-31 GHz)
- $P_{in} = P_{RFi} - L_1 + L_2 + L_4$ (dB)
- $P_{out} = P_{RFo} + L_3$ (dB)

$$PAE = (P_{out} - P_{in}) / P_{DC}$$

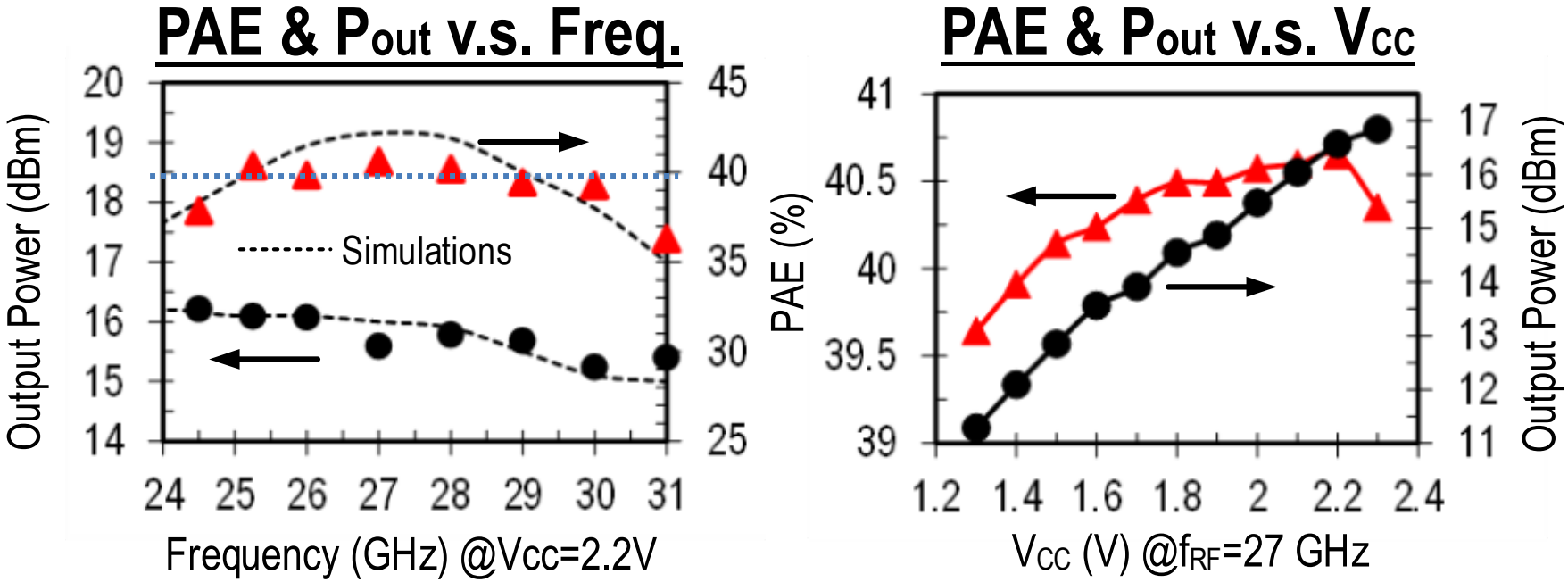
Large-Signal Performance (1)



Measurement @27 GHz

- Class-AB biasing (V_{CC}=2.2, I_{CE}=9mA)
- Peak PAE: 40.7% (Drain η: 52.7%)
- P_{sat}: 17.1 dBm (50 mW)
- OP_{-1dB}: 15 dBm

Large-Signal Performance (2)



- PAE: 39.3-40.7% @ 25-30 GHz
- PAE > 36% @24-31 GHz

Note: due to mode-transition, the PA can maintain ~40% PAE over 25-30 GHz.

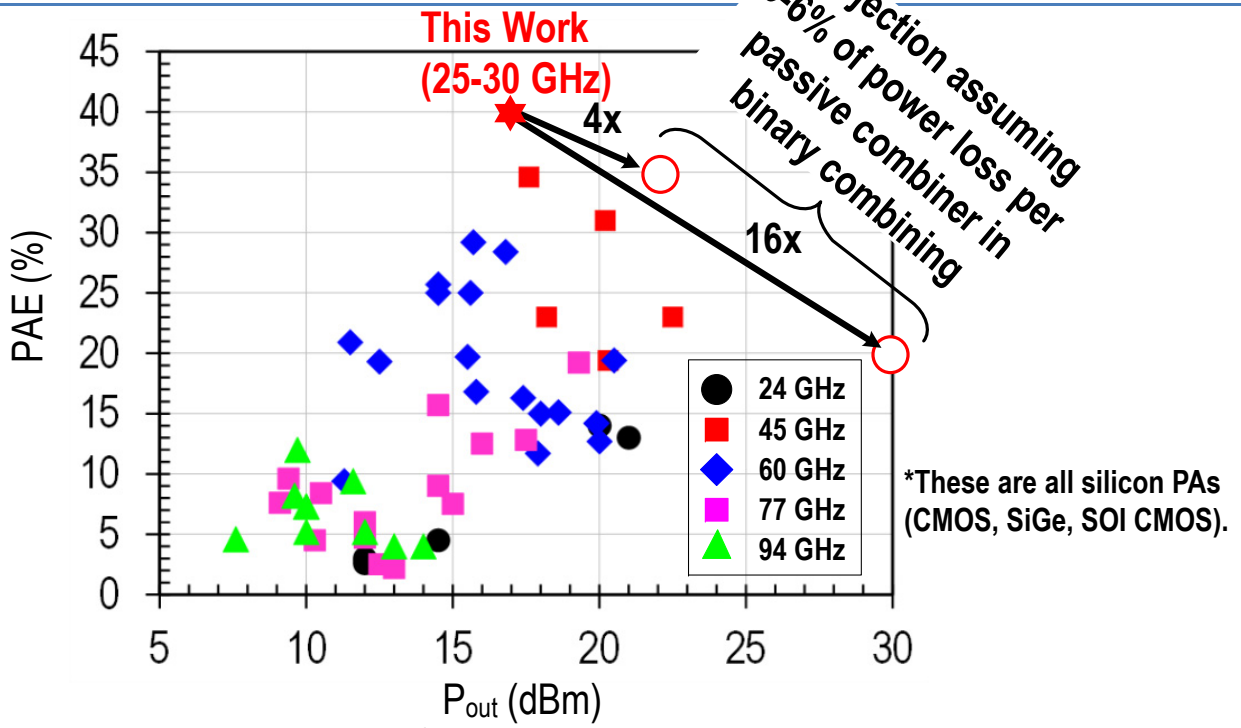
- PAE: 39.6-40.7% @ V_{CC}=1.3-2.3 V

Note: it can maintain ~40% PAE over 1-V V_{CC} variations with ~6-dB P_{out} variations.

Performance Summary & Comparison

Authors	Freq.(GHz)	PAE (%)	P_{sat} (dBm)	OP_{-1dB}(dBm)	Gain (dB)	Size (mm^2)	Supply(V)	Process
This Work	**25-30** **24-31**	**39.3-40.7** **36.3-40.7**	**17.1**	**15**	**10.3**	**0.27(0.14*)** *** w/o pad**	**2.2**	**0.13μm SiGe**
JSSC 2005 A. Komijani, *et al.*	24	6.5	14.5	11	7	1.26	2.8	0.18μm CMOS
RFIC 2007 M. Chang, *et al.*	33	11.2	17	15.5	13	1.83	1.4	0.13μm SiGe
JSSC 2005 T.S.D. Cheung, *et al.*	22 24	19.7 13	20-23	NA	15-19	6	1.8	0.2μm SiGe
RFIC 2005 N. Kinayman, *et al.*	24	2.9	12	11	18	1.1	5	0.5μm SiGe
T-MTT 2012 N. Kalantari, *et al.*	38	20	23	NA	18.7	1.04	3	0.12μm SiGe
CICC 2012 A. Chakrabarti, *et al.*	47	34.6	17.6	NA	13	0.12	2.5	45nm SOI CMOS
CICC 2012 K. Datta, *et al.*	45	31.5	20.2	NA	10.5	1.3	2.4	0.13μm SiGe
T-MTT 2012 P.-C. Huang, *et al.*	24-26	40	23.5	22	9	1.5	4	GaAs HEMT
RFIC 2013 N. Kinayman, *et al.*	26.4	38	25.3	NA	10.3	25	5	GaAs HEMT
MTTs 2012 C.F. Campbell, *et al.*	29	30	37	NA	25	4.8	20	GaN HEMT

Conclusion



- First successful silicon PA in Class-F^{-1} and Class-F at mm-wave with a record ~40% peak PAE at 25-30 GHz.
- First successful realization of a mode-transition mm-wave PA to achieve a high PAE over a wideband: 24-31 GHz (25.5% fractional BW) with PAE > 36%.
- A linear mode (Class-AB) PAE with 6-dB back-off is ~26%, still comparable to peak PAE of state-of-the-art silicon PAs.
- With 16x power combining, potentially it can achieve > 20% PAE with Watt-level P_{out}.

Acknowledgements

- DARPA program, *Silicon Based Phased Array Tiles for Multifunctional RF Sensors*, under a subcontract from University of California San Diego (UCSD).
- Prof. G. M. Rebeiz (UCSD) for financial and measurement support.
- Dr. M. Chang (Univ. Michigan), Fatih Golcuk (UCSD), and Hsin-chang Lin (UCSD) for help in PAE measurements.

A 0.53THz Reconfigurable Source Array with up to 1mW Radiated Power for Terahertz Imaging Applications in 0.13µm SiGe BiCMOS

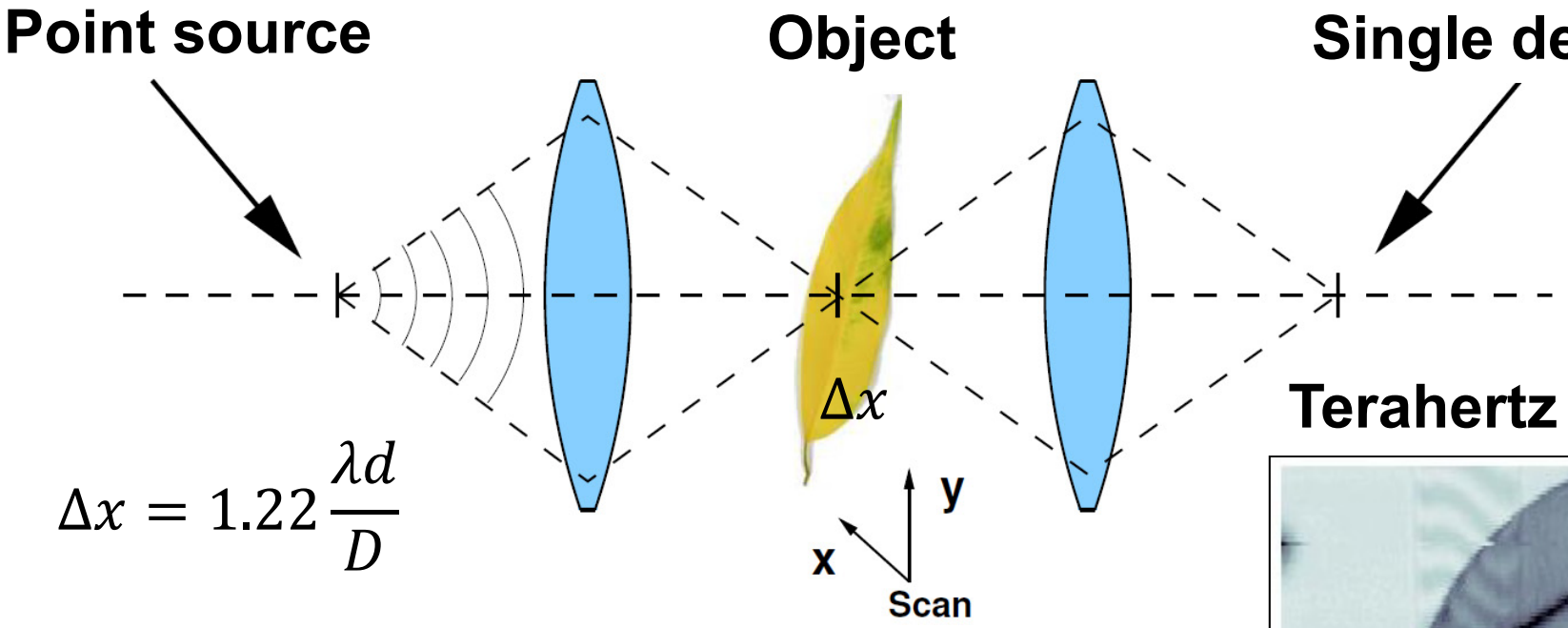
Ullrich R Pfeiffer[1], Yan Zhao[3], Janusz Grzyb[1], Richard Al Hadi[1], Neelanjan Sarmah[1], Wolfgang Förster[1], Holger Rücker[2], Bernd Heinemann[2]

[1]IHCT, University of Wuppertal, Germany
[2]IHP, Frankfurt (Oder), Germany
[3]was with [1] now with UCLA, Los Angeles, USA

Outline

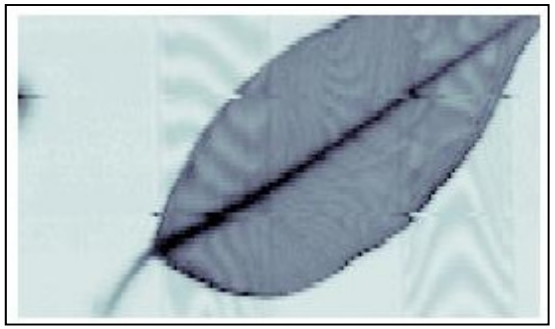
- Motivation
  - Diffuse illumination for terahertz imaging
- Source array architecture
- Oscillator circuit design considerations
  - Harmonic termination for maximum Pout
- Antenna design considerations
- Measured results
- Terahertz active imaging demonstration
- Conclusions

A “Poor Man's” THz Imaging System



$$\Delta x = 1.22\frac{\lambda d}{D}$$

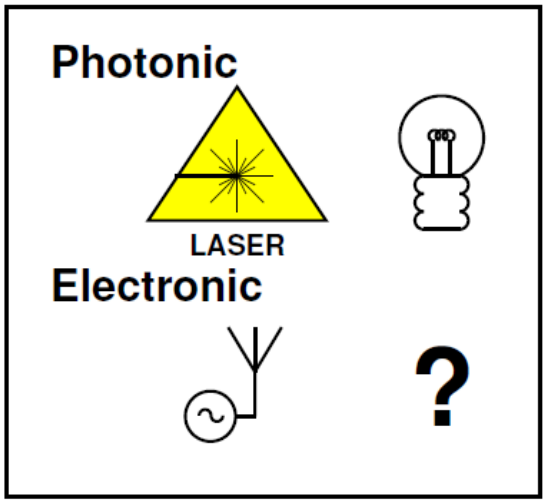
Terahertz image



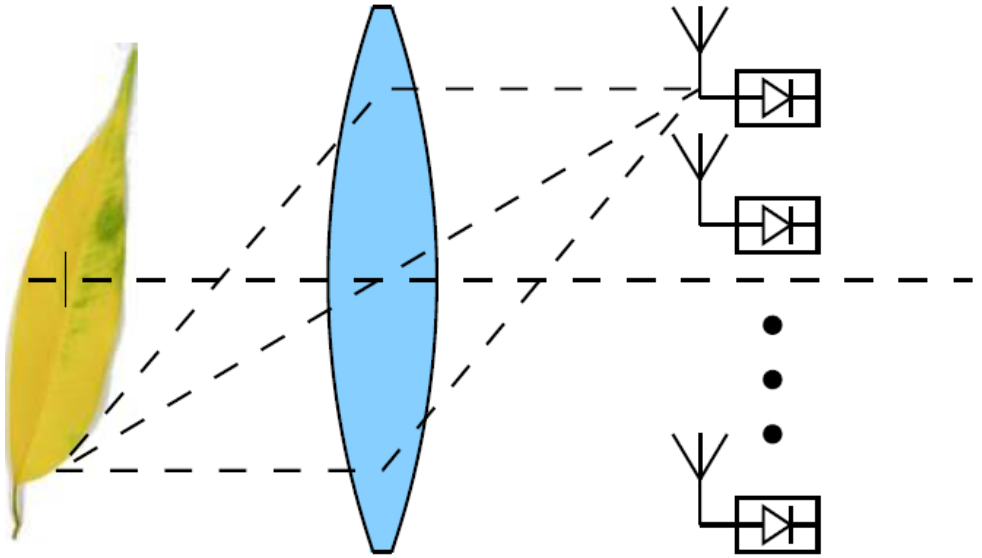
- Ambient (natural) THz radiation very weak
- Active illumination required to overcome limited detector sensitivity (no LNAs available)
- Limited source power requires focused illumination, e.g. scanner-based systems with back-channel (chopping)

How to use THz Video Cameras?

Which source?



Focal plane Array



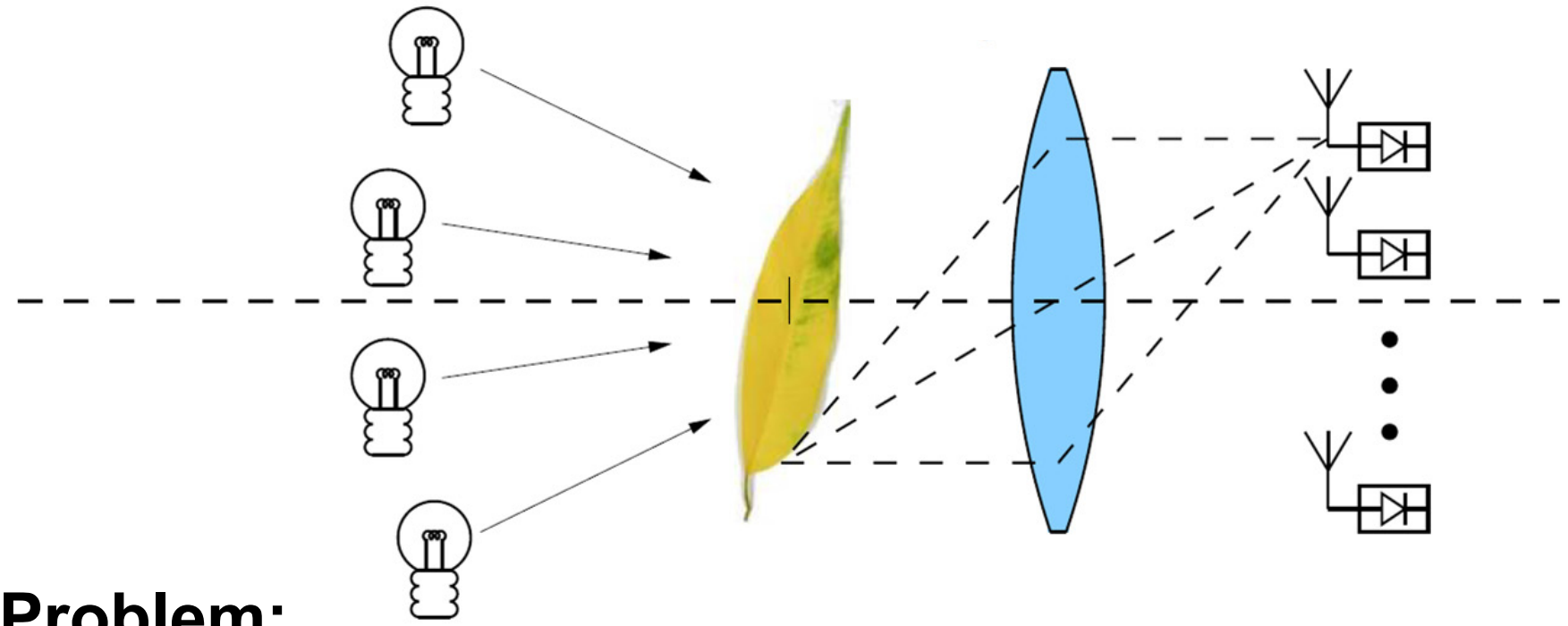
Problem:

FPAs require full illumination of the scene (all object points)

1st Option: defocus point source, but this substantially reduces the power density (low image SNR)

2nd Option: use more sources

Motivation – Diffuse Illumination



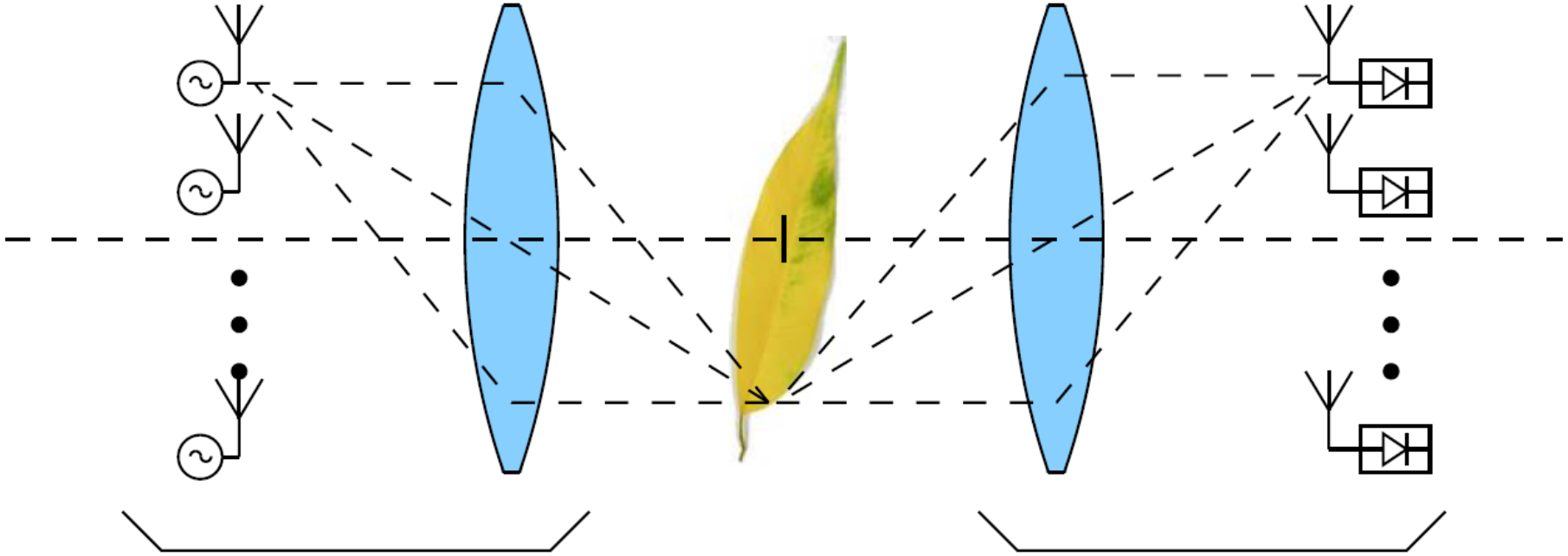
Problem:

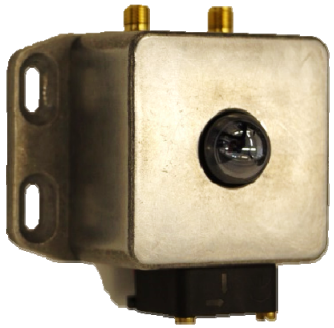
Illumination with coherent sources creates specular reflections

→ use defuse, uncorrelated illumination

→ use many oscillators with spatial diversity, ideal for silicon

THz Imaging with Source Module

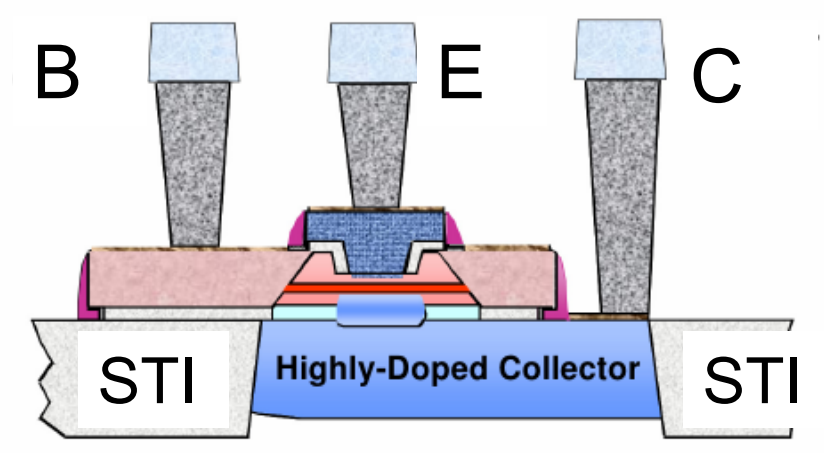


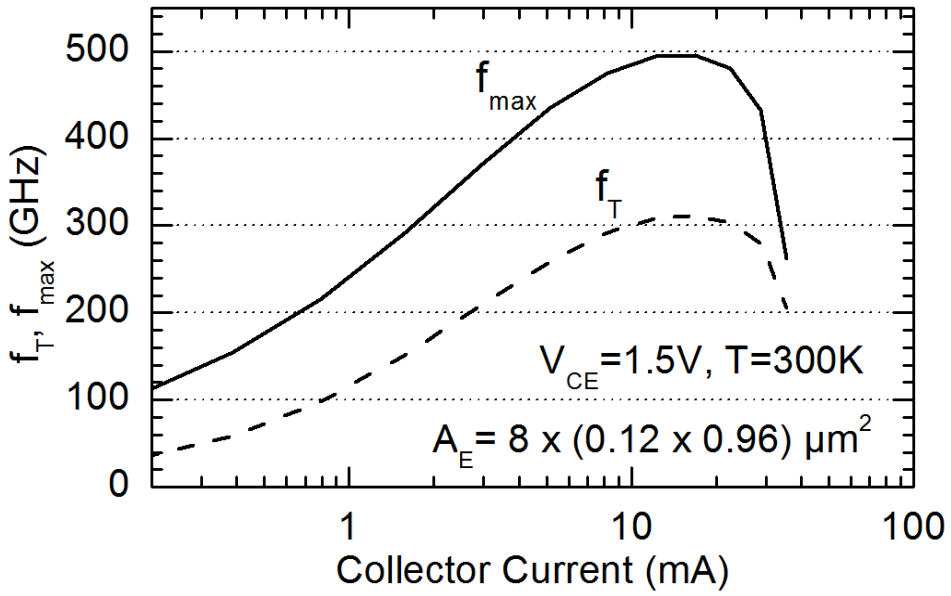


no synchronization

Sherry et al.
ISSCC12

Used SiGe HBT Technology

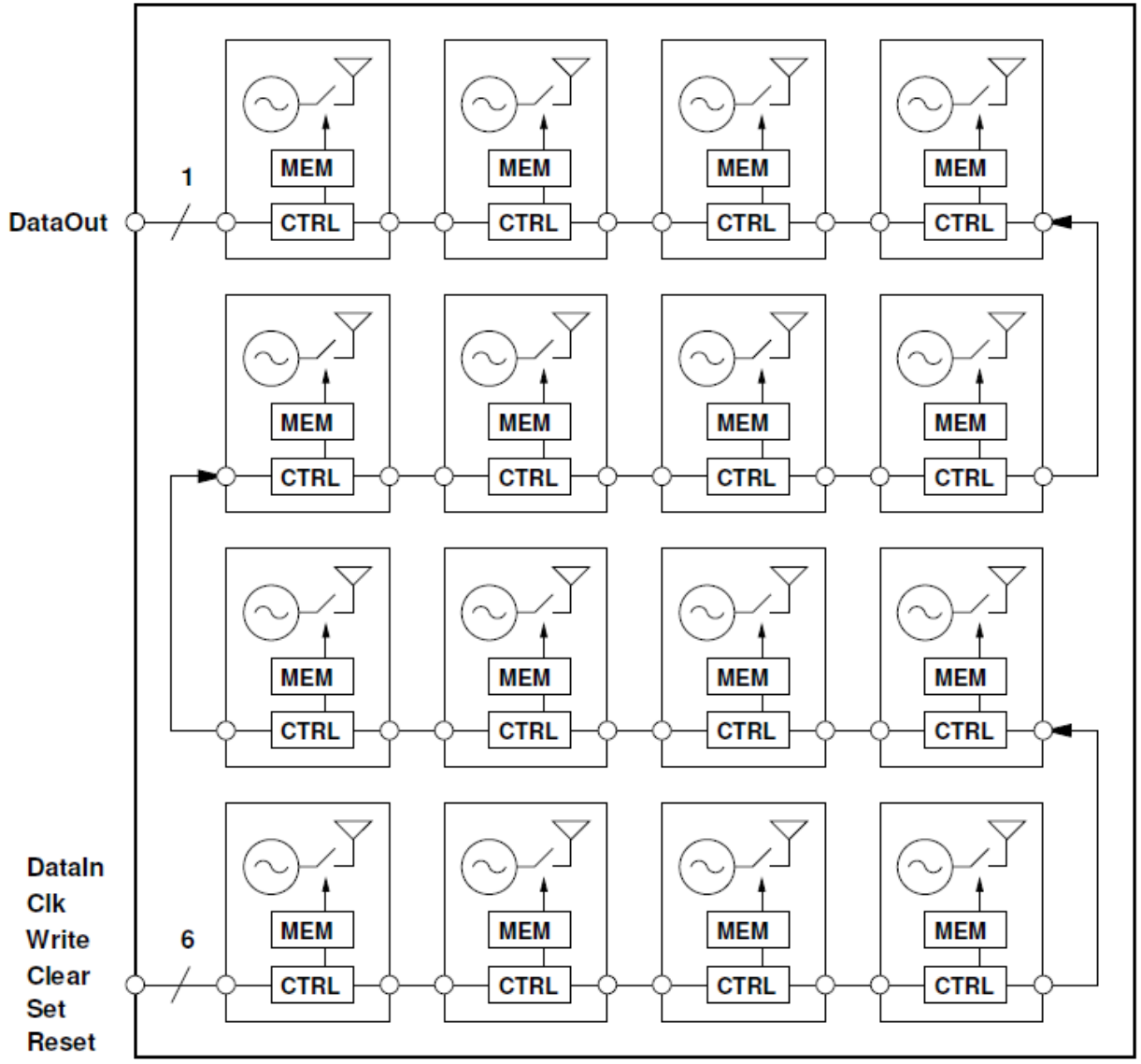




Technology Features

- IHP 0.13µm BiCMOS SG13G2 flow
- HBT with elevated extrinsic base self-aligned to emitter window
- Based on DOTFIVE results of f_T/f_{max}= 300GHz/500GHz [Heinemann IEDM 2010]
- BV_{CEO} = 1.6V
- Current gain ~650

Circuit Block Diagram



- 4x4 pixel source array with adjustable lighting condition
- Synchronous latched shift register in meander-type structure
- Circuit layout scalable in size and output power
- 16 output registers drive TPO power-down switch, configurable at runtime
- Fully integrated including on-chip antennas

Source Pixel Block Diagram

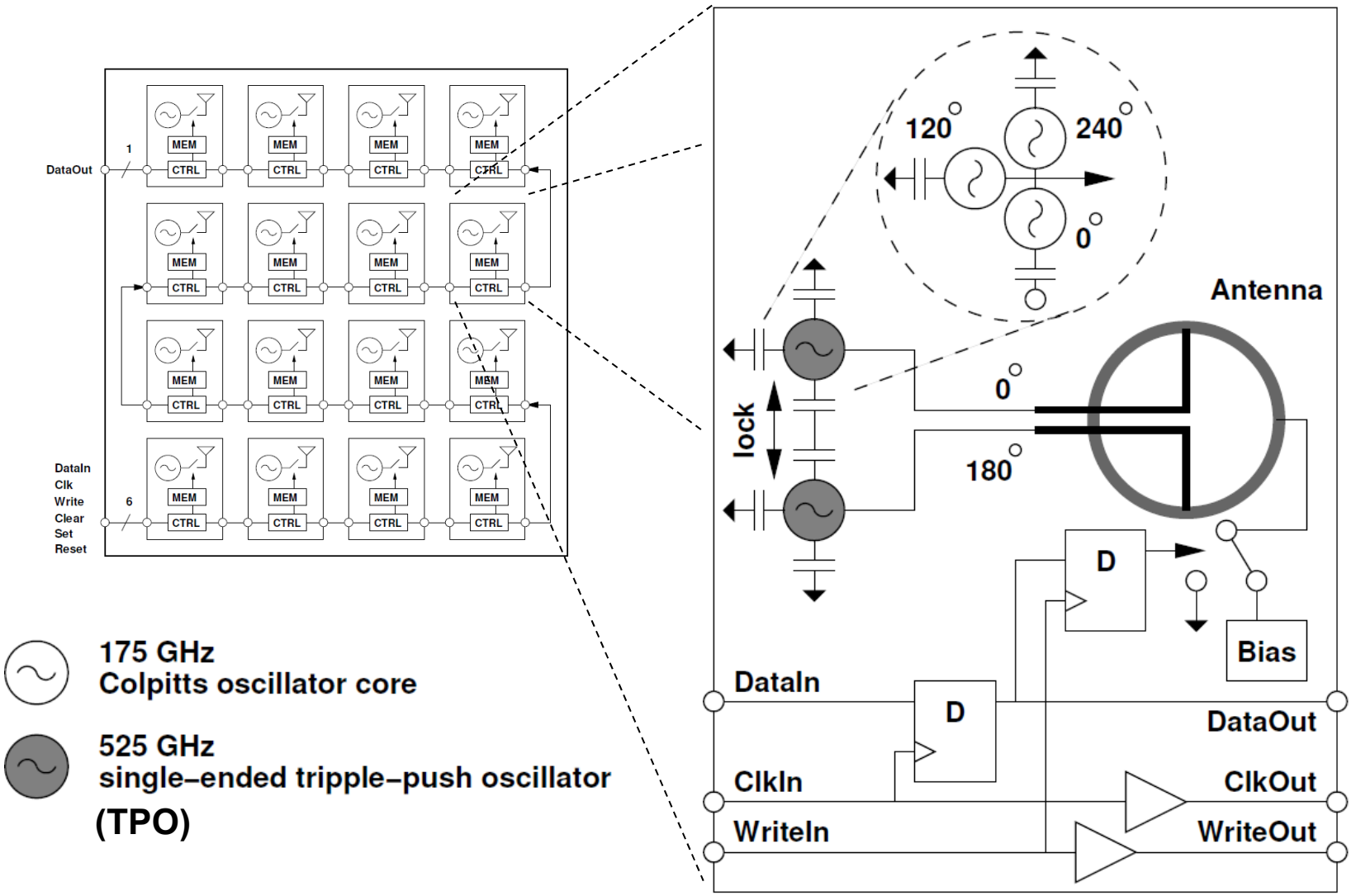


Illustration of the Locking Method

Fundamental Phase Diagrams

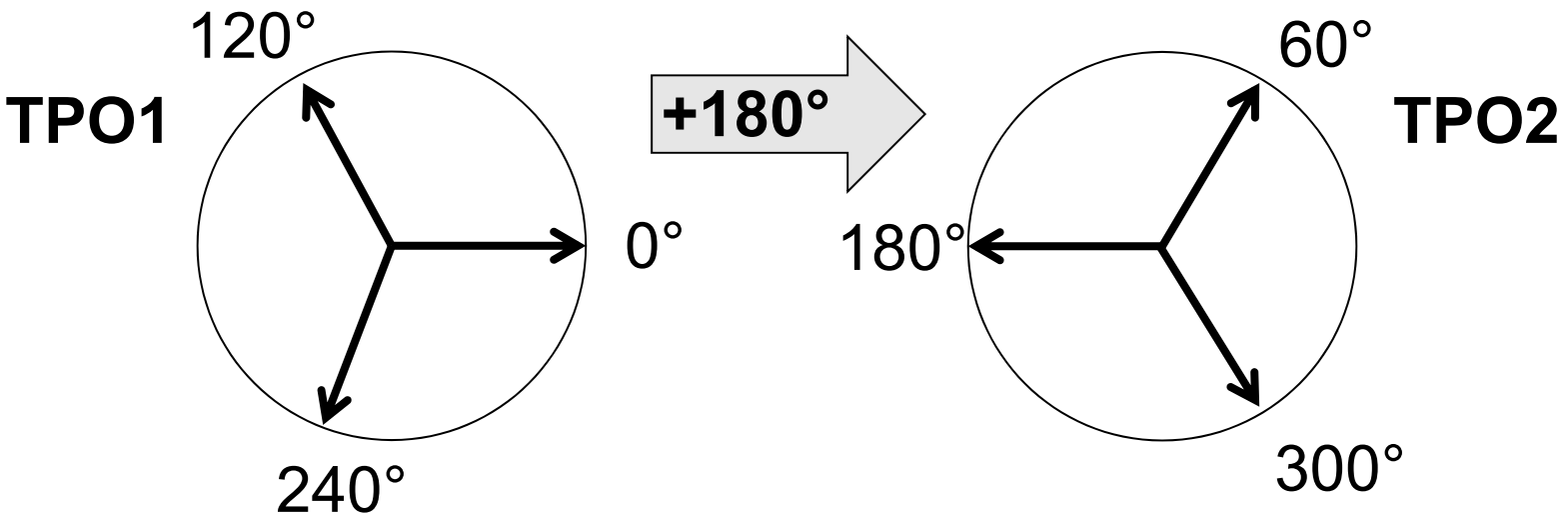
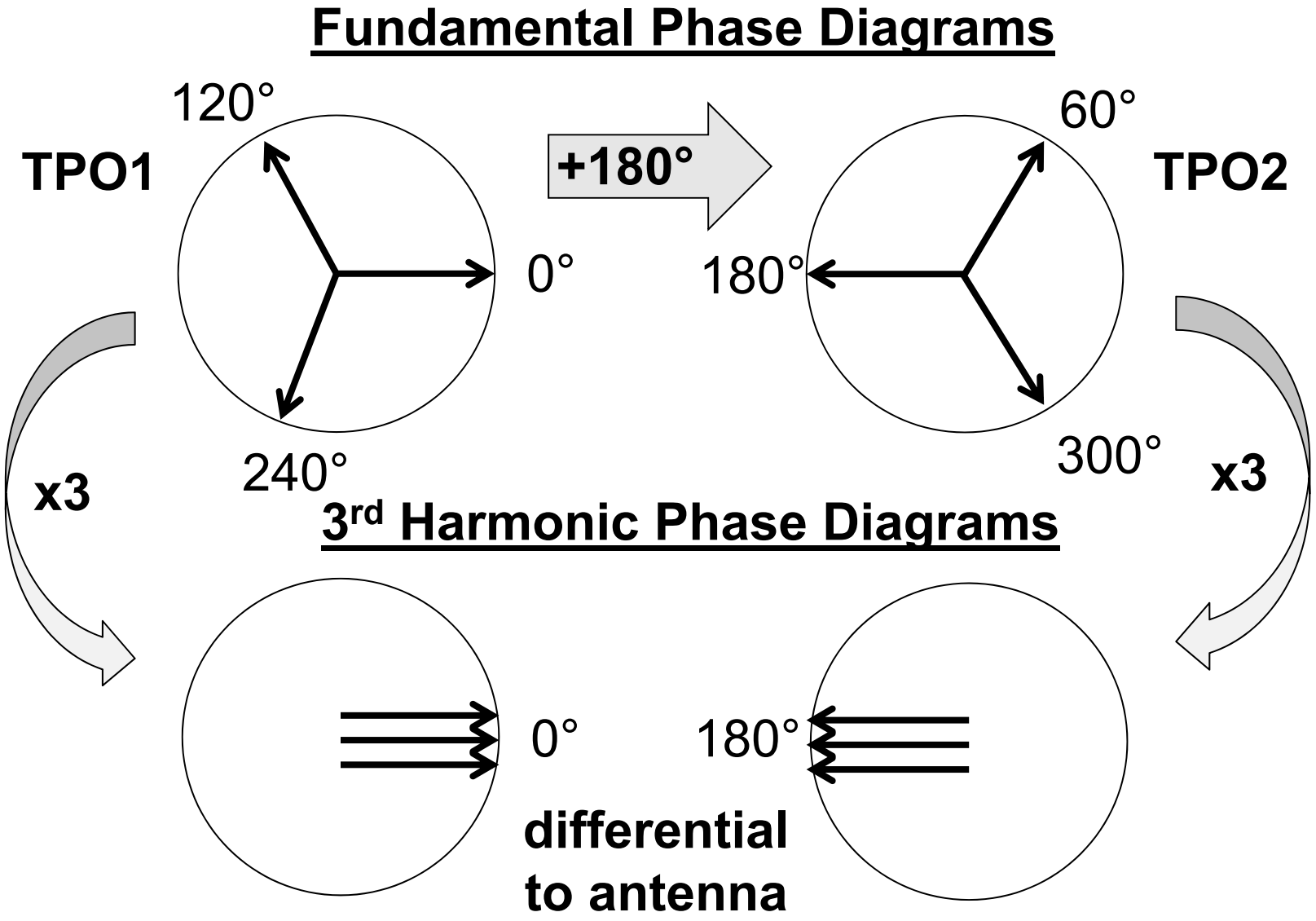


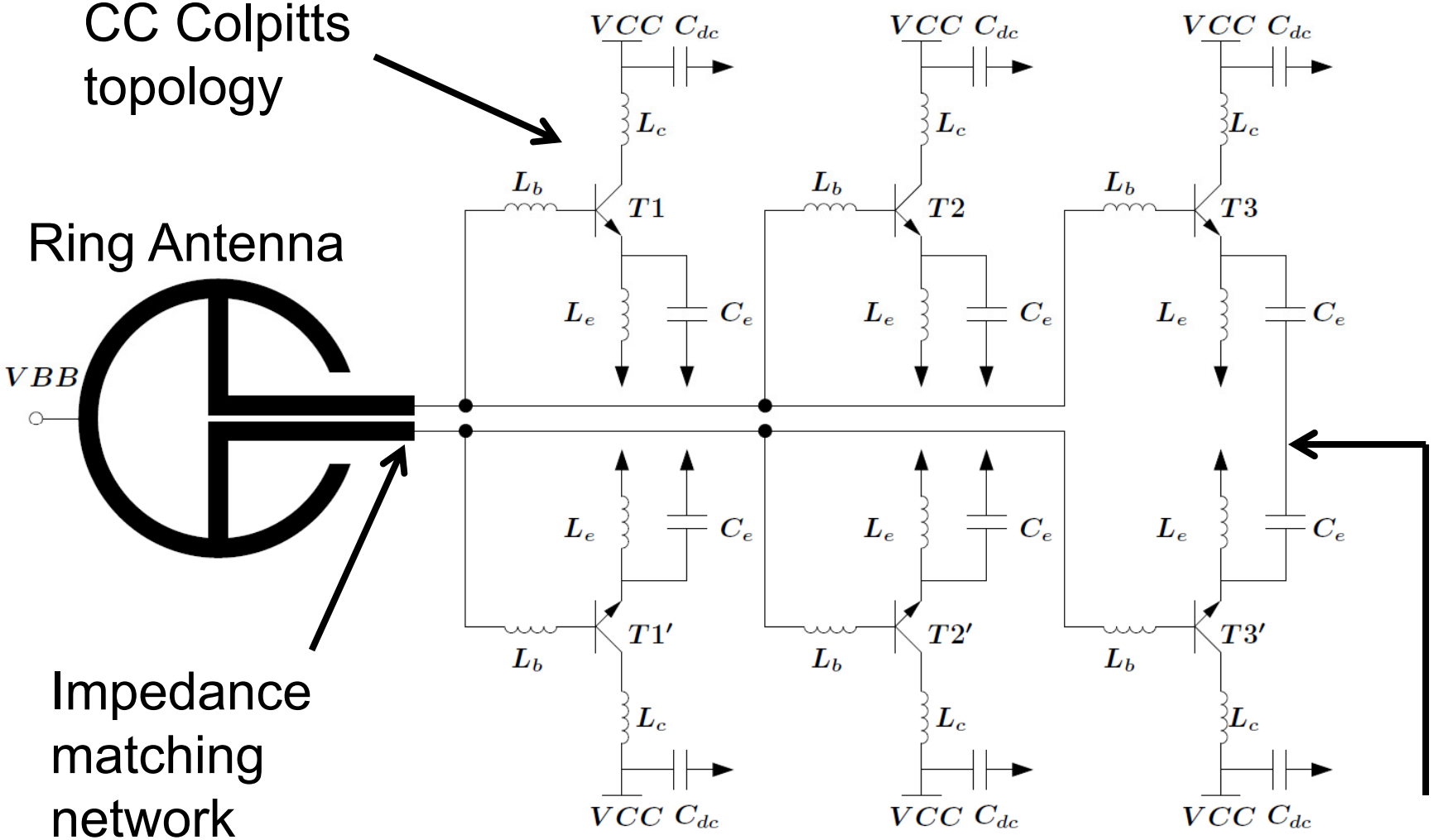
Illustration of the Locking Method



Core TPO Circuit Schematic

CC Colpitts topology

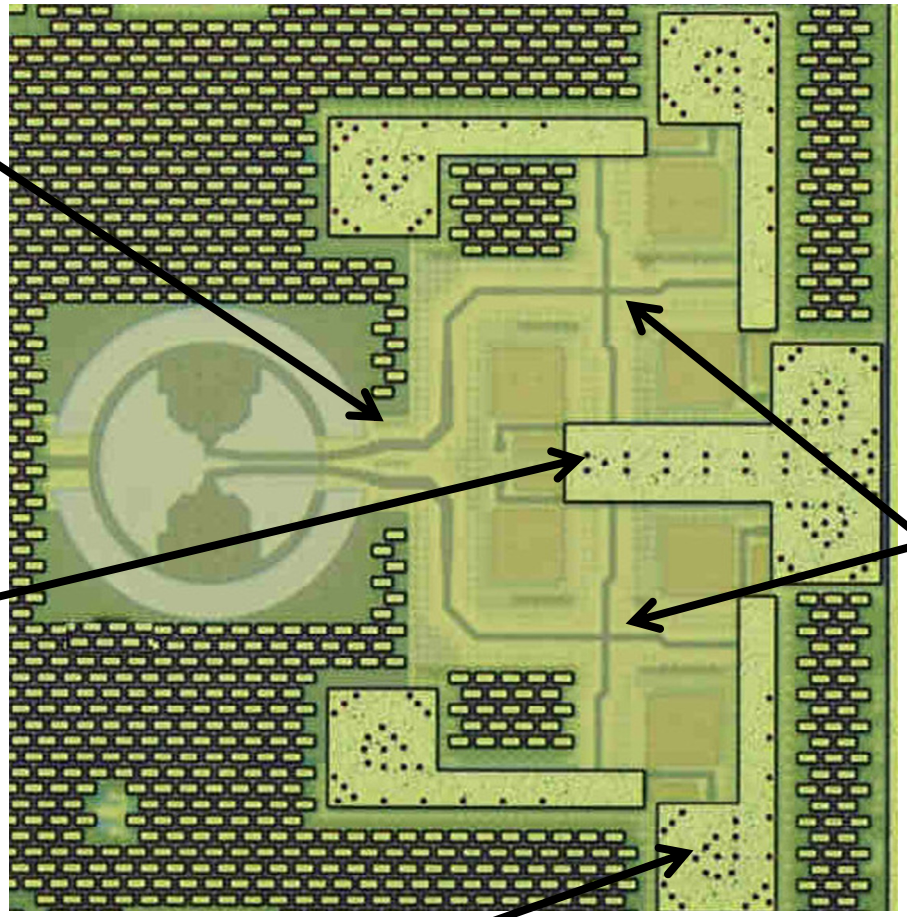
Ring Antenna



Impedance matching network

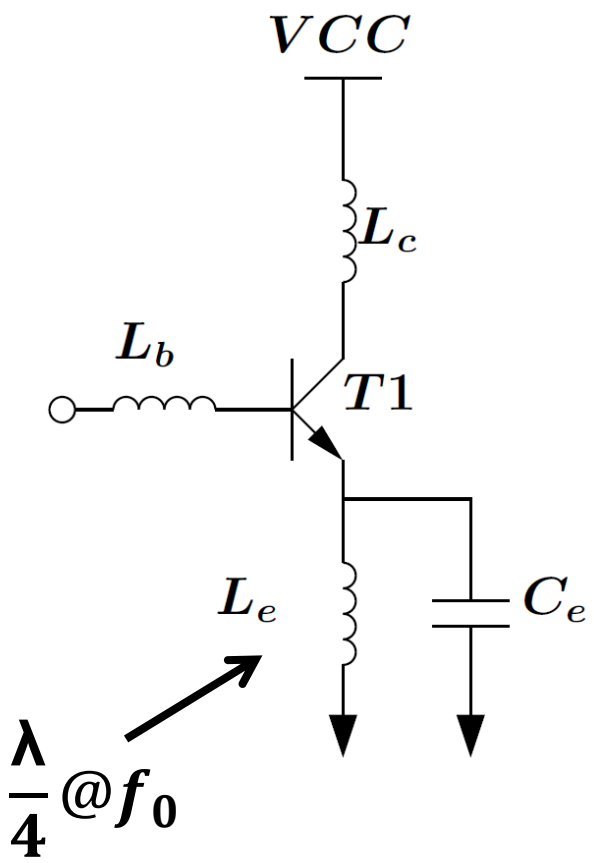
TPOs locked 180deg out of phase to drive antenna

Single Source Pixel Micrograph



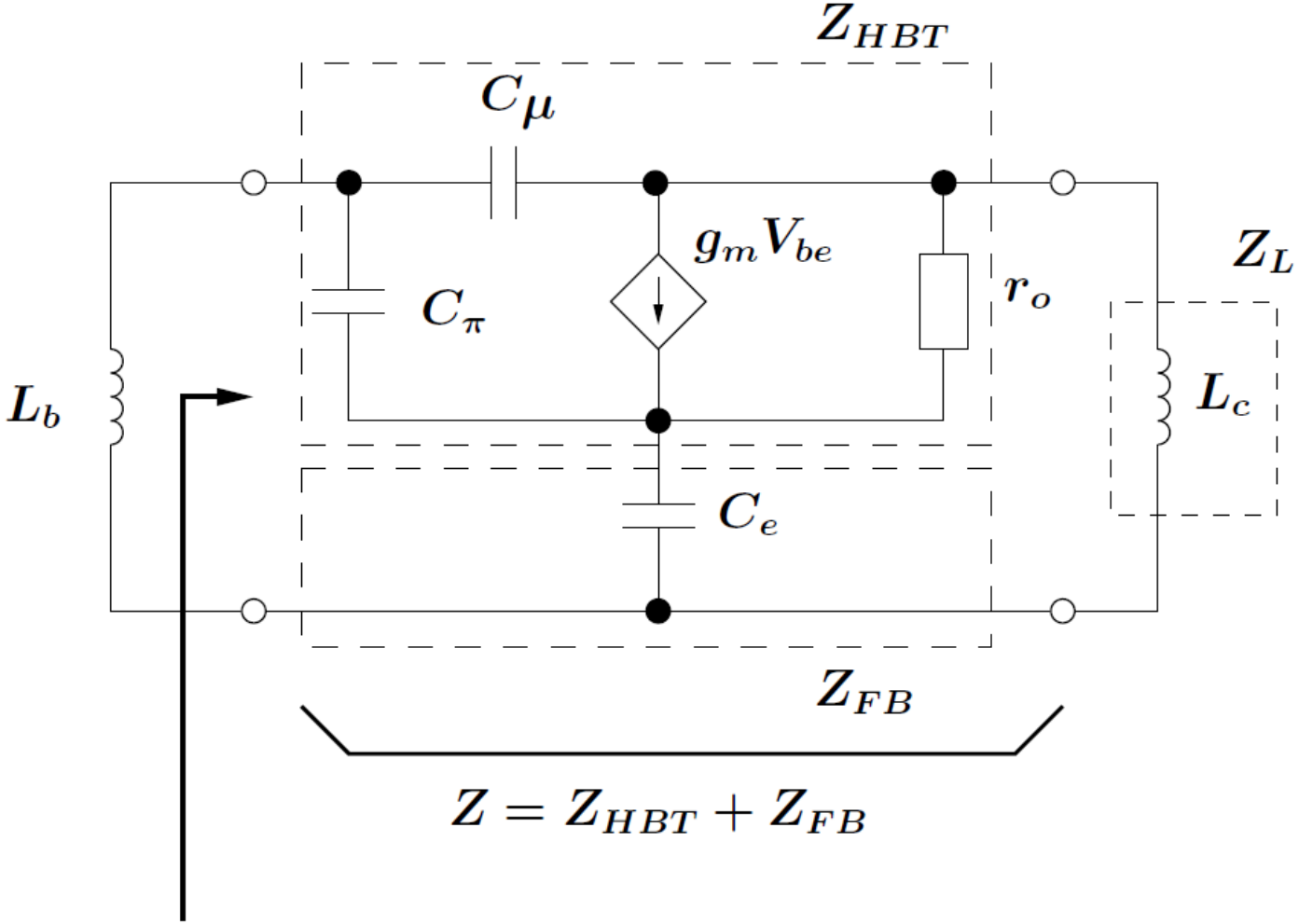
Circuit Design Considerations

Single Colpitts



- 3rd harmonic beyond f_{max}
  - → Extraction of 3rd harmonic from base-emitter diode directly
  - → Use CC Colpitts vs. CB, CE topology
  - → Use L_C for waveform shaping at base node
- Select fundamental f_0=175GHz
  - → Tank is tuned by base inductor L_b
  - → C_π is fixed by the device size
  - → C_e creates neg. resistance through series feed back
- Relevant Harmonics
  - → 1st: 175 GHz (diff. mode)
  - → 2nd: 350 GHz (common mode)
  - → 3rd: 525 GHz (diff. mode)
  - → 4th: 700 GHz (common mode)

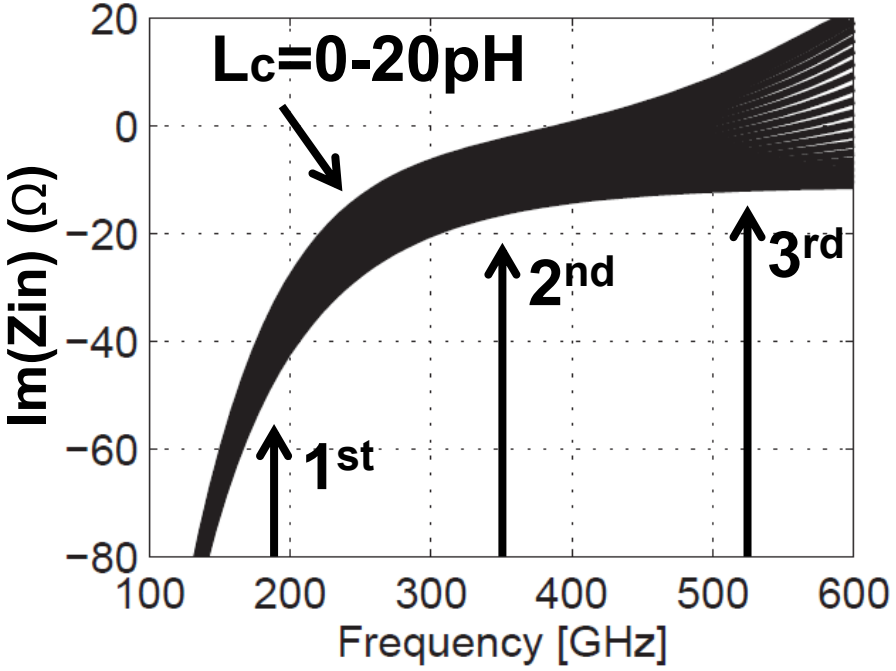
Small Signal Analysis (Single Colpitts)

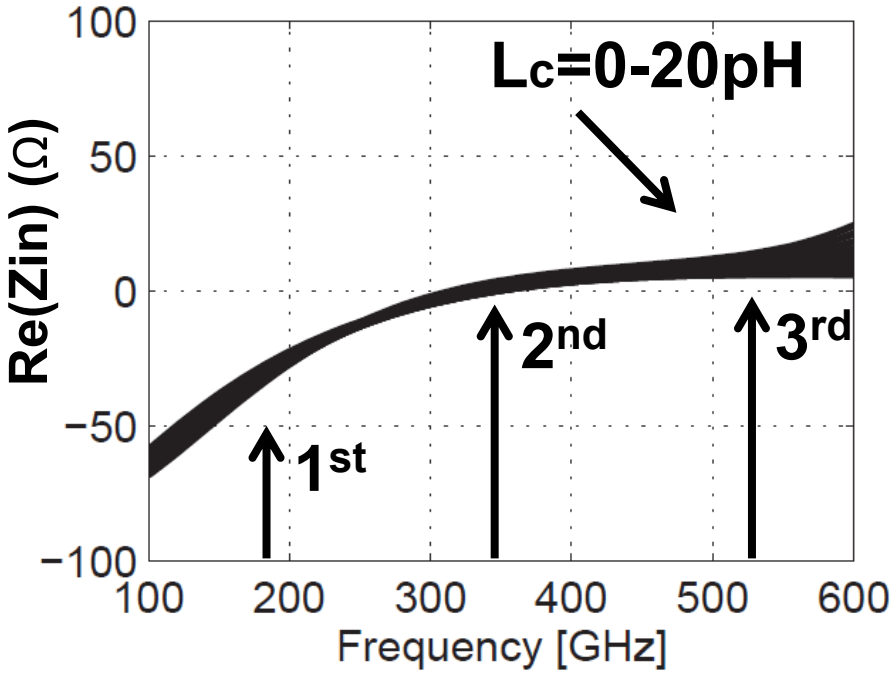


$$Z_{in} = Z_{11} - \frac{Z_{21} Z_{21}}{Z_{22} + Z_L}$$

@175GHz (VBIC)	
Cμ	8 fF
Cπ	22.5 fF
ro	500Ω
Ce	13 fF
Lb	40 pH
Lc	10 pH
gm	0.03 S
Ae	5x0.07x0.9 μm²
β	650
Ic	6.738 mA
VCC	1.5 V
Vbe	0.9 V

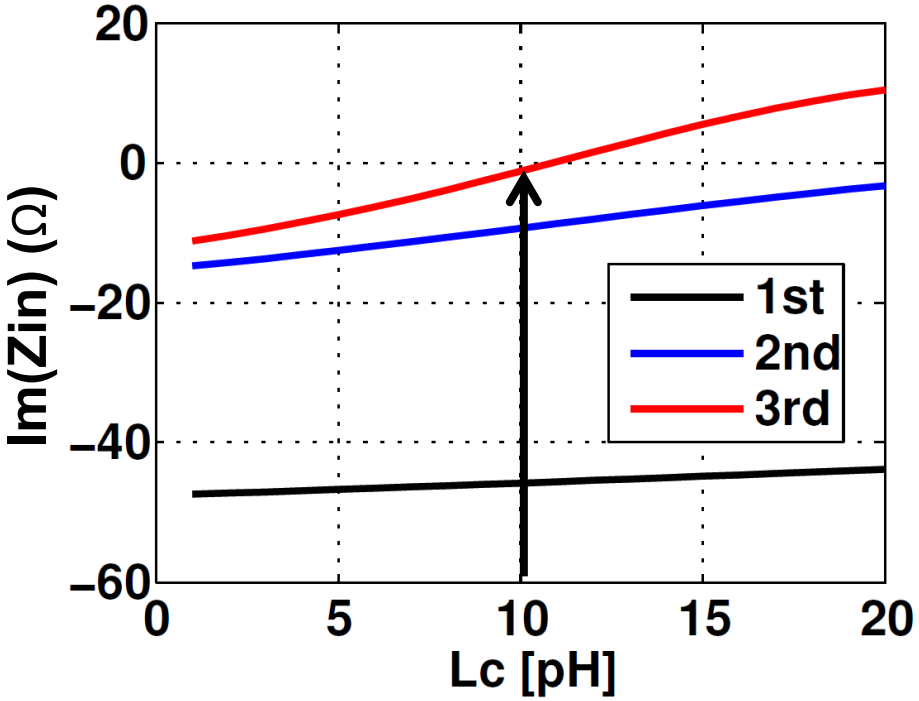
Impact of L_c Tuning on Z_{in} (Sim.)

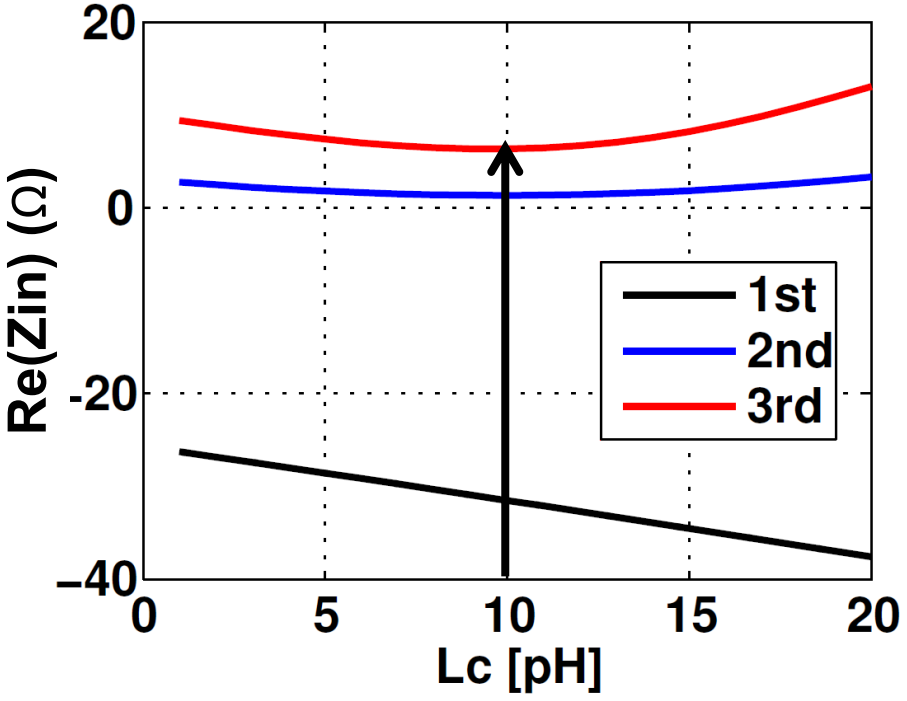




- Marginal impact on 1st harmonic reactance
- Large impact at 3rd harmonic reactance
  → Tune out reactance and match for power extraction
- Marginal impact on real part (all harmonics)

Optimum Lc Tuning (Sim.)



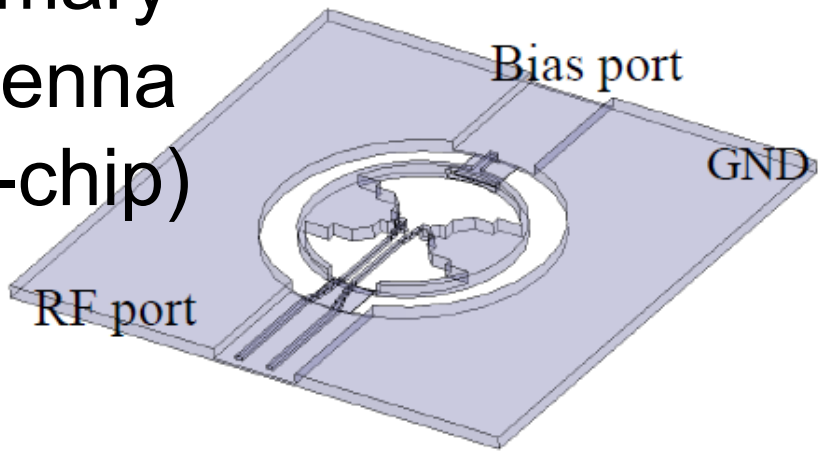


Optimum Lc=10pH (single-ended, half-circuit):

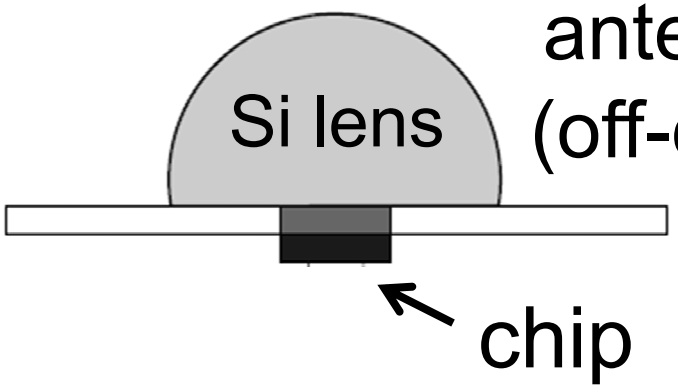
3rd harm. (525GHz)	Zin=	8 Ω	→ real load
2nd harm. (350GHz)	Zin=	0 -j10 Ω	→ harmonic short
1st harm (175GHz)	Zin=	-30 -j45 Ω	→ neg. resistance

Ring Antenna Design

Primary antenna (on-chip)



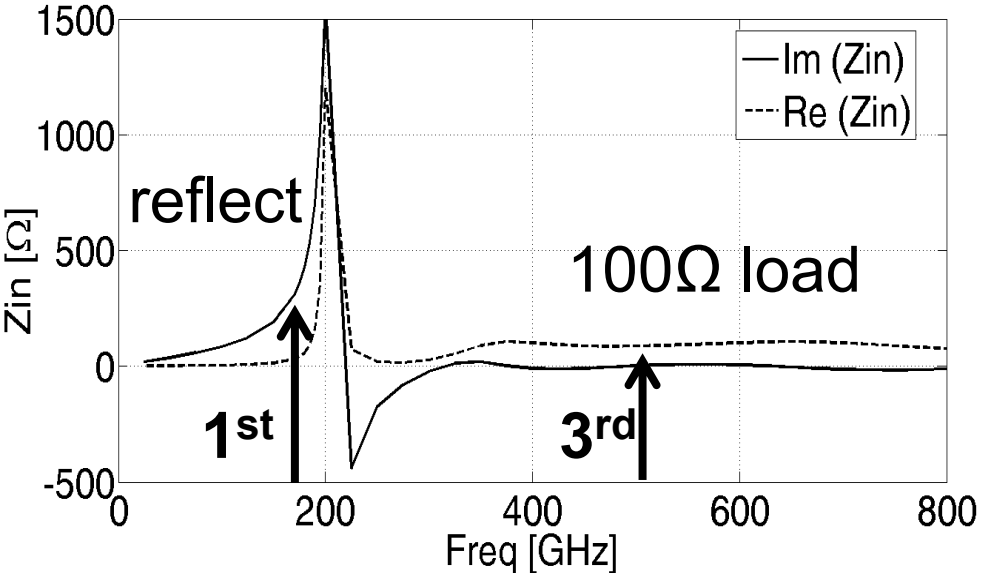
Secondary antenna (off-chip)



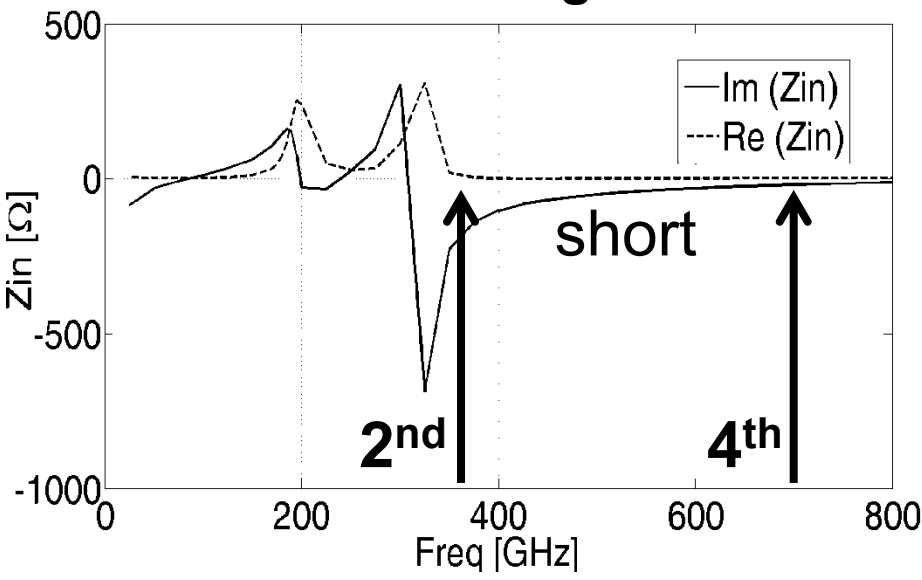
- Silicon lens reduces chip area up to factor of 3, element spacing $\lambda/2$ is reduced by $1/\sqrt{\varepsilon_r}$
- Silicon lens is detachable, size may depend on application
- Radiation through the Silicon lens reduces Substrate-modes
- Simulated radiation efficiency is 85% at 520GHz (HFSS)
- Inter-element coupling is -35dB from 350 to 800GHz
- 15mm lens diameter, 37dBi (FWHM) at 525GHz

Ring Antenna Impedance Match

Differential signals

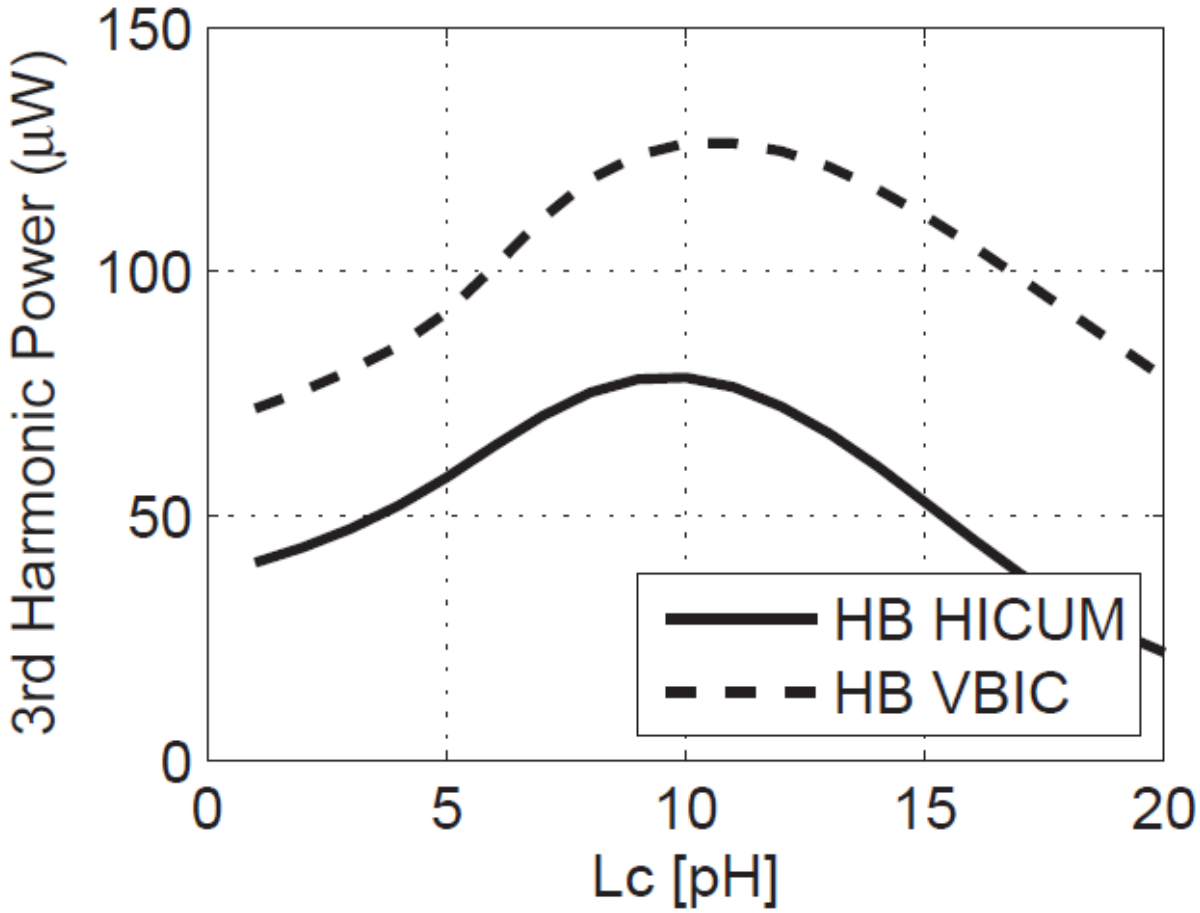


Common-mode signals



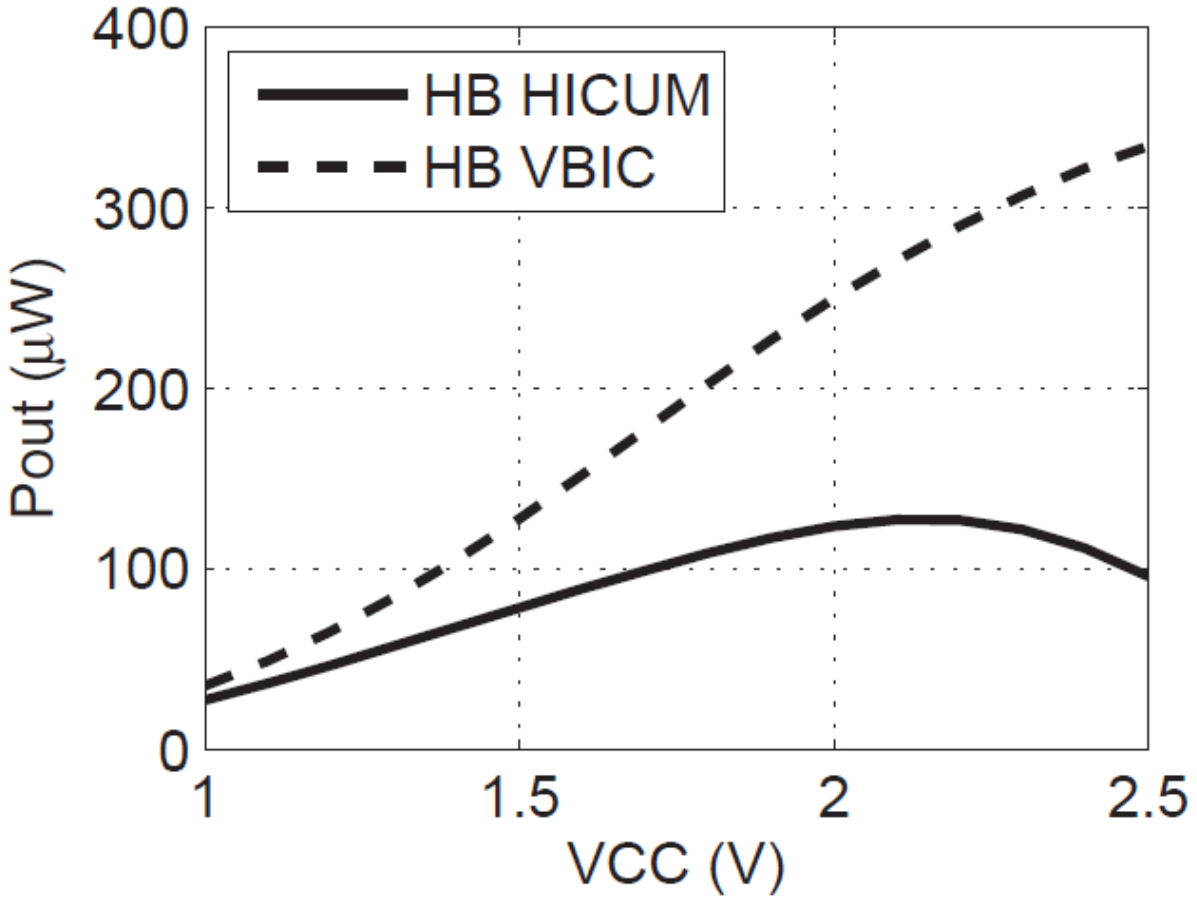
- Differential impedance (relevant for odd harmonics)
  - Very high and reactive at the fundamental (reflect at 1st harmonic)
  - 100Ω load from 360-800GHz (100Ω termination at 3rd harmonic)
- Common-mode impedance (relevant for even harmonics)
  - Real short from around 330-800GHz (short at 2nd and 4th)
  - High and reactive at the fundamental (reflect at 1st harmonic)

Single TPO Output Power vs. Lc (Sim.)



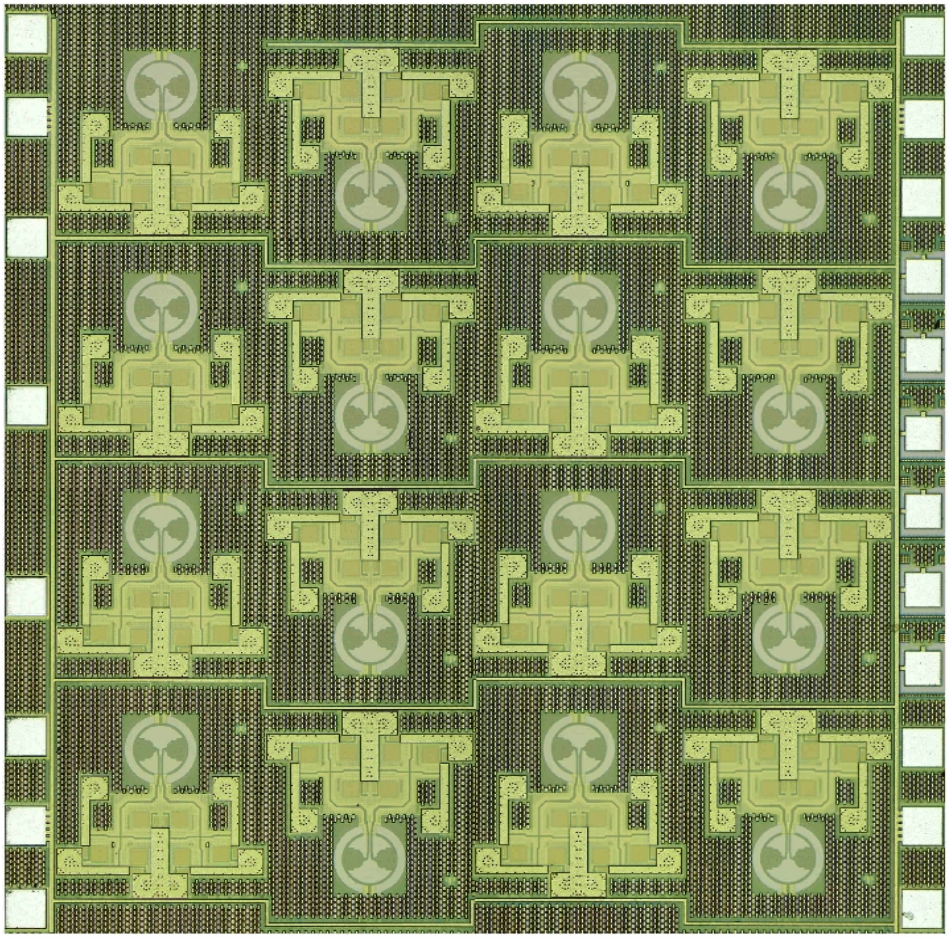
- 3rd harmonic power is maximized for L_C=10pH
- 2dB difference between HICUM/VBIC device model

Single TPO Output Power vs. VCC (Sim.)



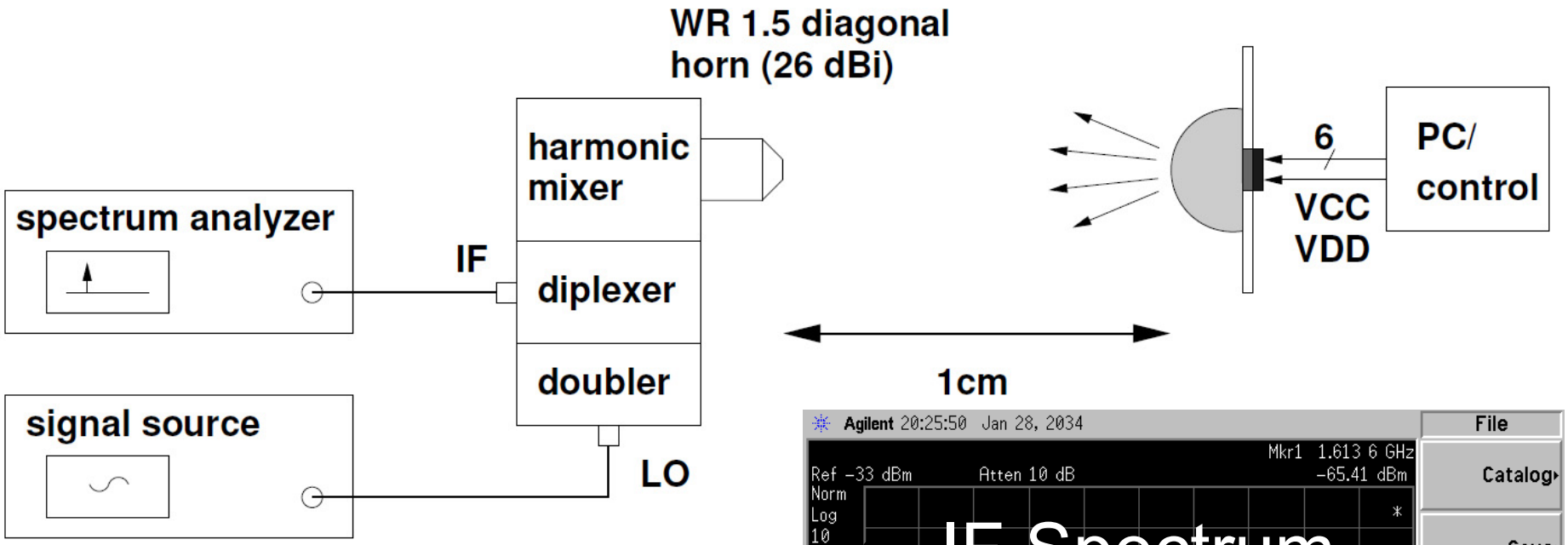
- Up to 5dB difference between HICUM/VBIC device model
- High current effects better modeled with HICUM
- Expected differential Pout = -9dBm+3dBdiff -loss > 100μW

Chip Micrograph

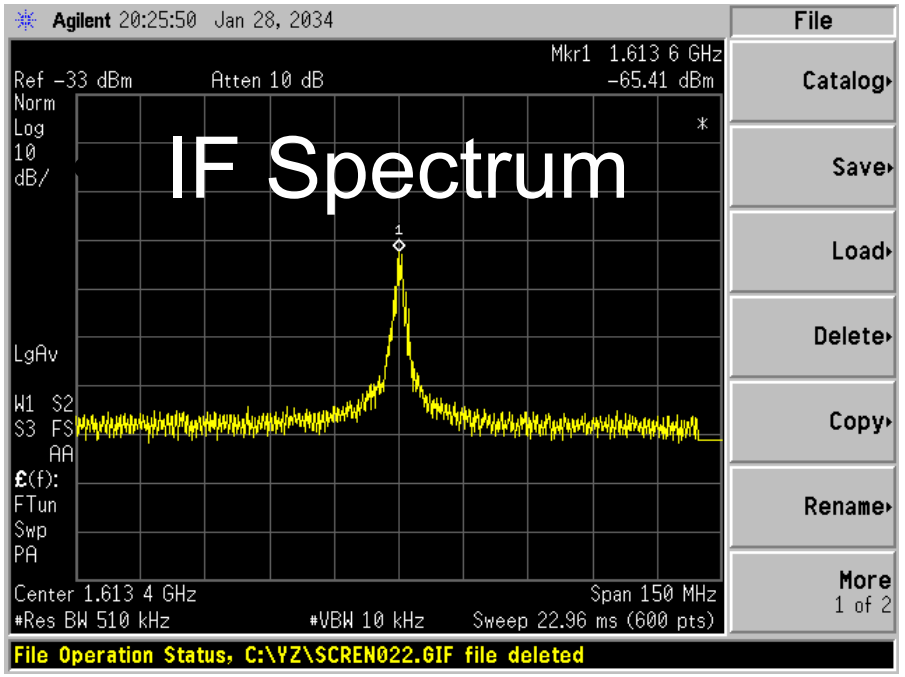


- Honeycomb tessellation to save die area
- Total die area of 2x2.1mm^2 for all 16 source pixel
- 510µm pitch

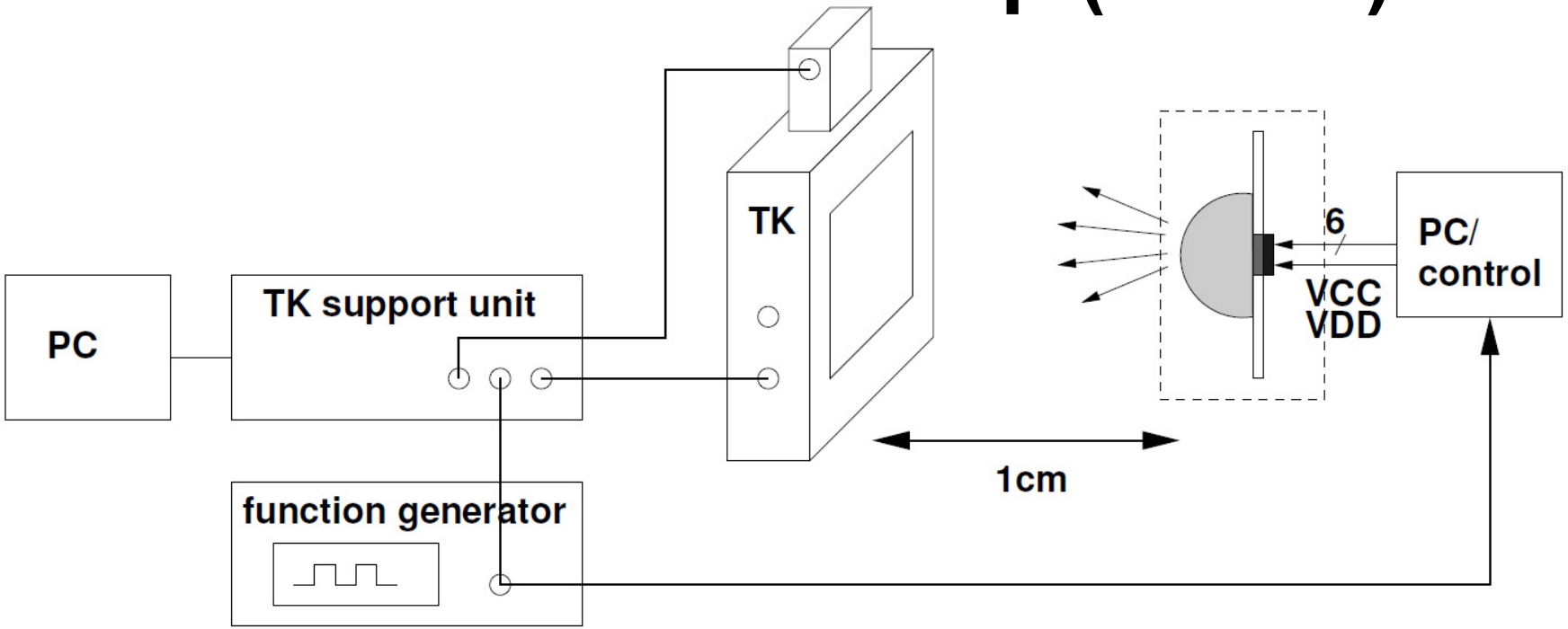
Measurement Setup (Spectrum)



- Used to measure oscillation frequency of each pixel
- Each pixel has frequency offset

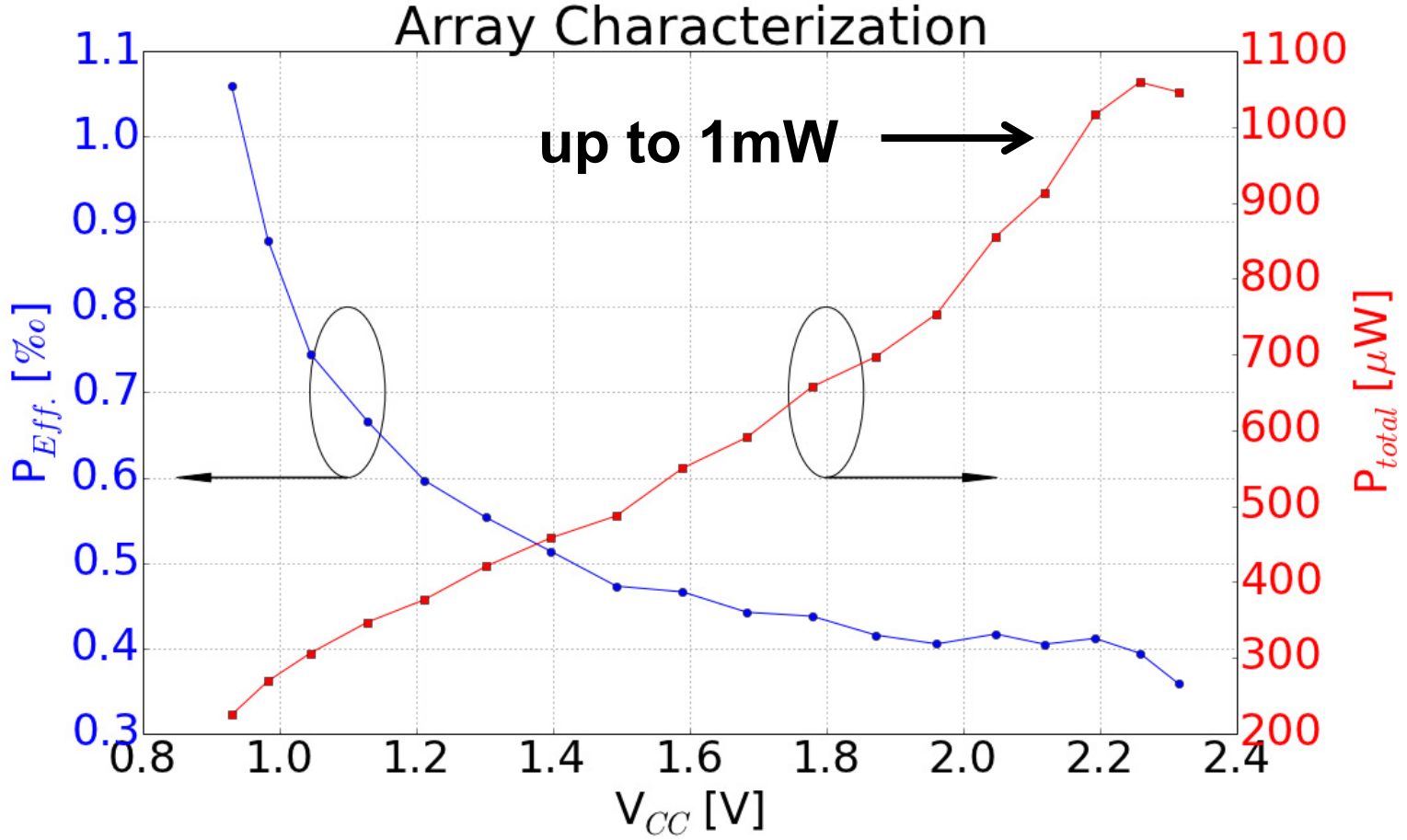


Measurement Setup (Power)



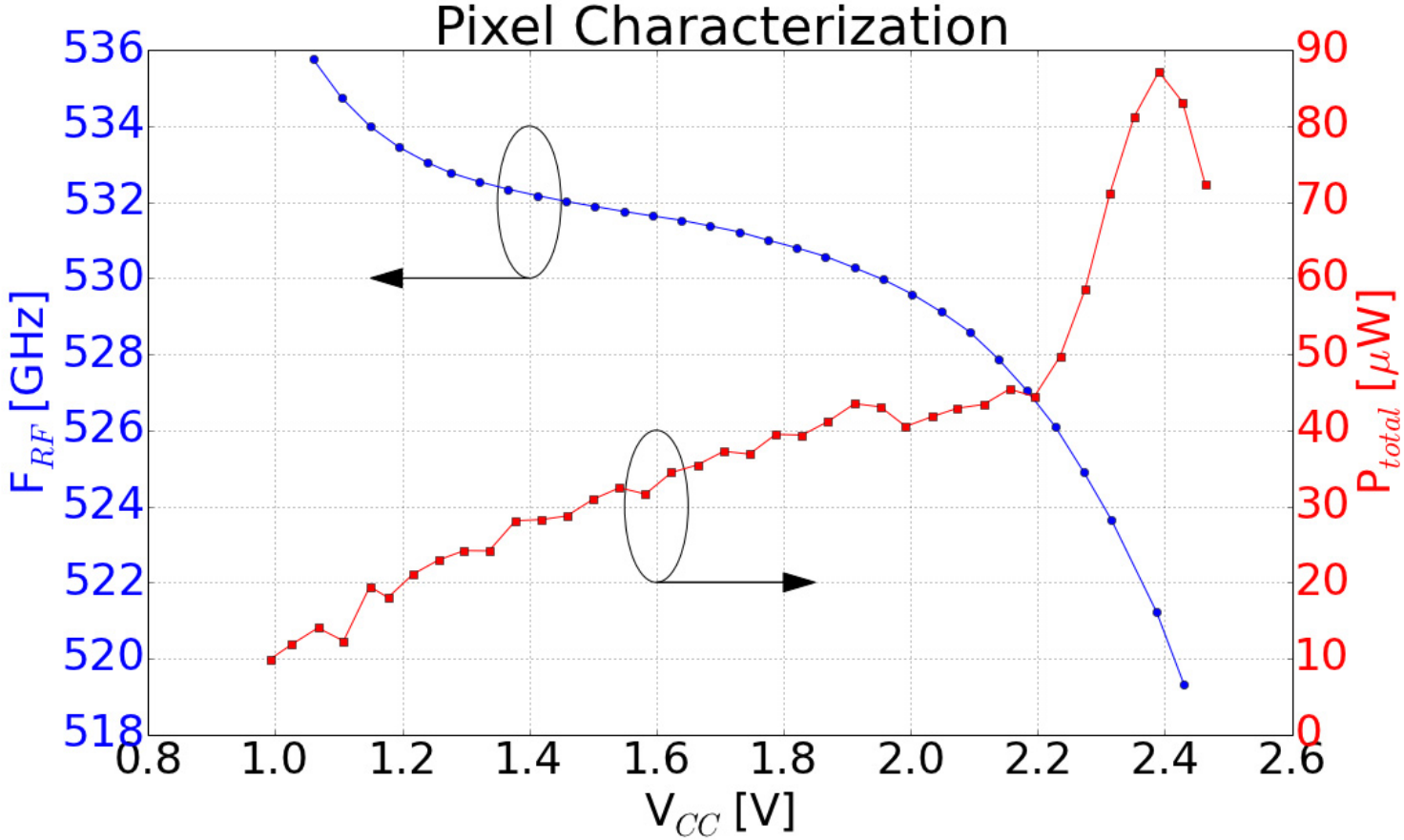
- Measured with photo-acoustic absolute power meter (TK)
- Includes harmonic leakage power
  - Estimated to be a few % (~10μW) based on a breakout TPO measured in the D-band
- Source chopping required due to thermal emission background (2.5W DC from 2.5V)
  - Electronic chopping available though serial interface

Measured Total Power (all on)



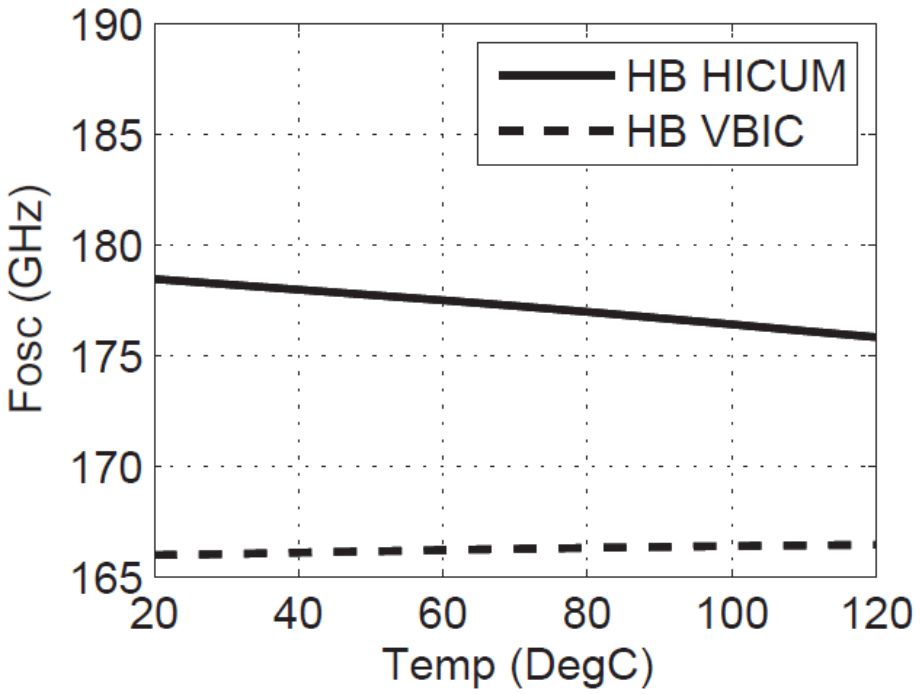
- Full array can deliver up to 1mW (0dBm) RF power
- DC to RF conversion efficiency is 0.4 to 1‰
- Draws up to 2.5W from a 2.5V supply

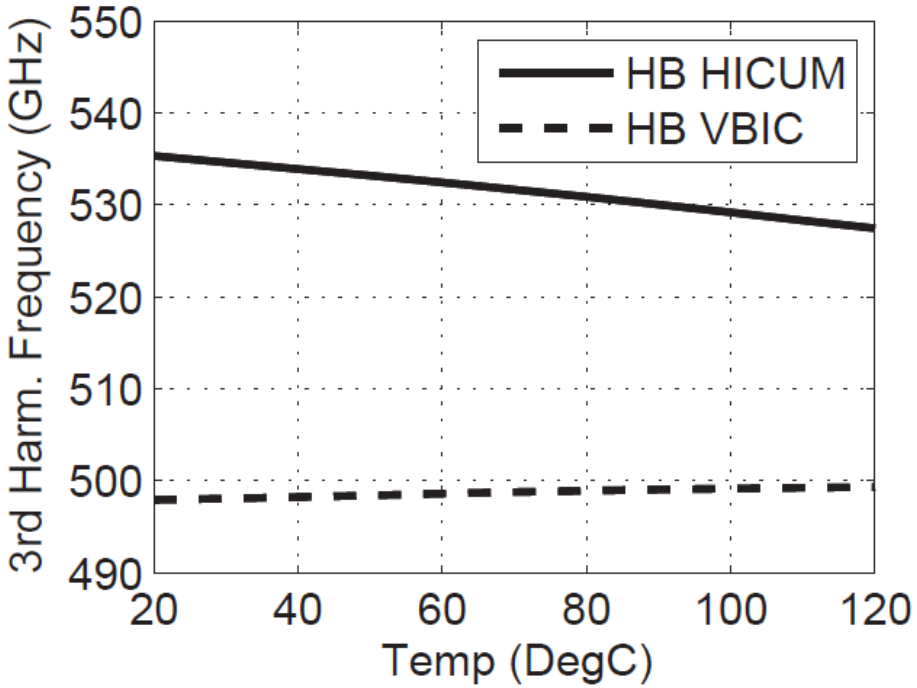
Measured Single Source Pixel



- Single pixel provides up to 85µW (26dBm EIRP)
- F_{OSC} drops due to thermal self-heating
- Single pixel draws about 150mW @2.5V

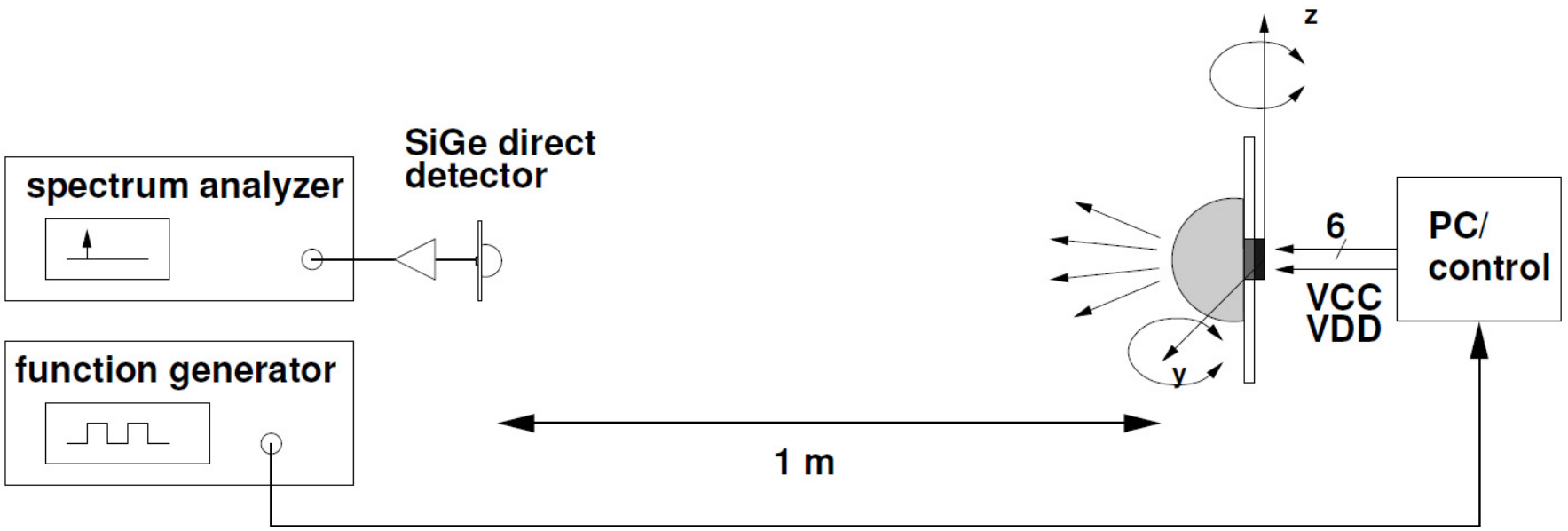
Simulated Fosc vs. Temperature





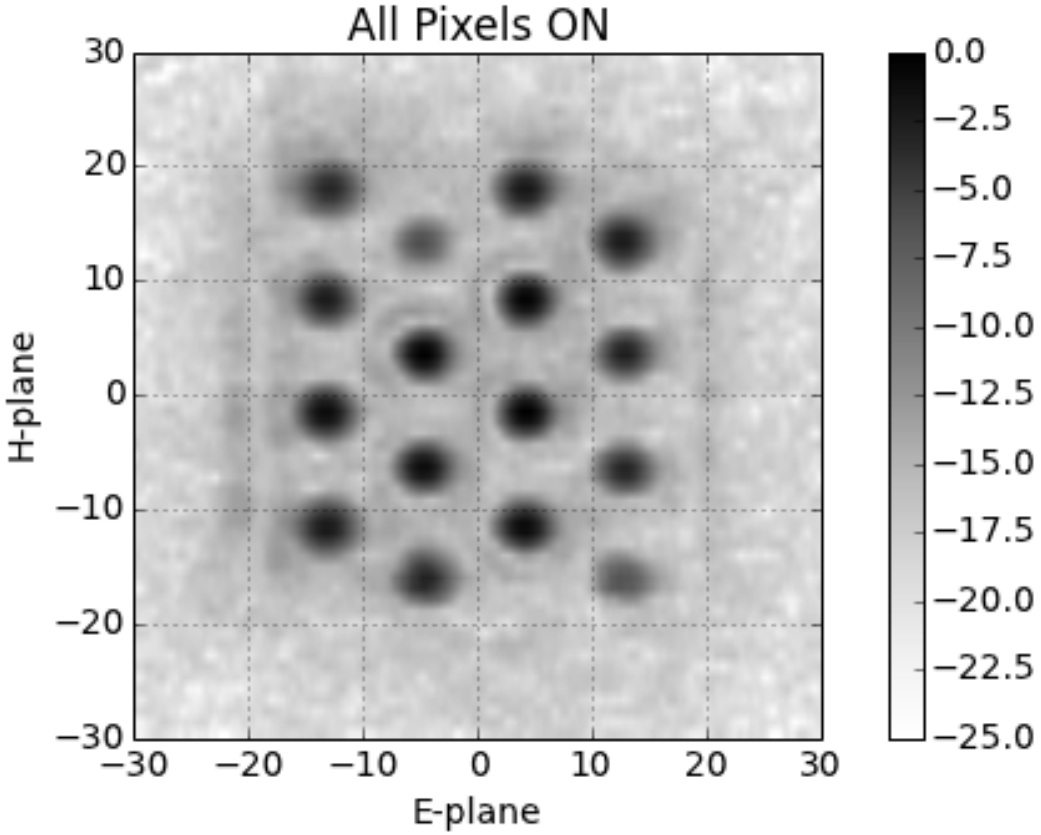
- Simulation of self-heating at high currents predictable by HICUM device model
- Simulated temperature coefficient (100MHz/K) matches measurements

Measurement Setup (Ant. Pattern)



- Source array mounted on rotational joint at a 1-m far field
- SiGe lens-coupled square-law detector used as RX
- Electronic source chopping available through serial interface

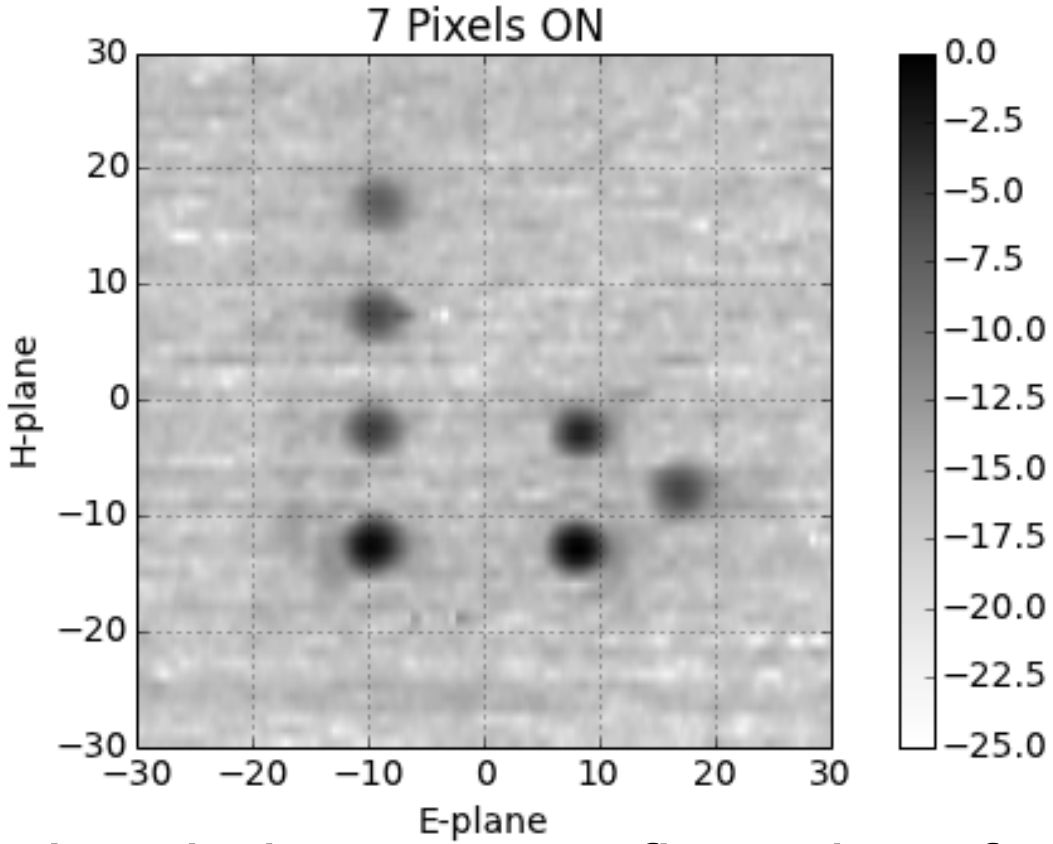
Measured Antenna Patterns



- Pattern depend on the secondary antenna
- Other lenses can be used to fit application requirements
- Side lobes are 15dB down

- Loaded source configurations for 16, 7, 4, and 1pixel
- Power down switching time is 0.5ns
- 16 beams cover a ±15º field-of-view

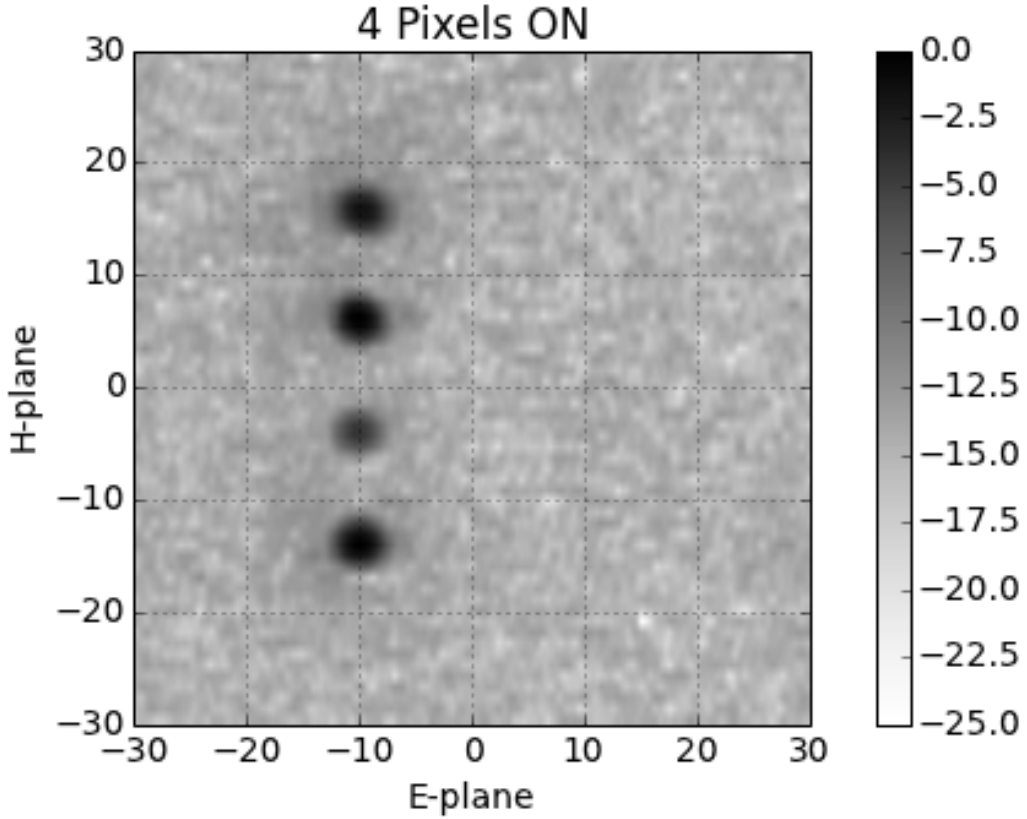
Measured Antenna Patterns



- Pattern depend on the secondary antenna
- Other lenses can be used to fit application requirements
- Side lobes are 15dB down

- Loaded source configurations for 16, 7, 4, and 1pixel
- Power down switching time is 0.5ns
- 16 beams cover a ±15º field-of-view

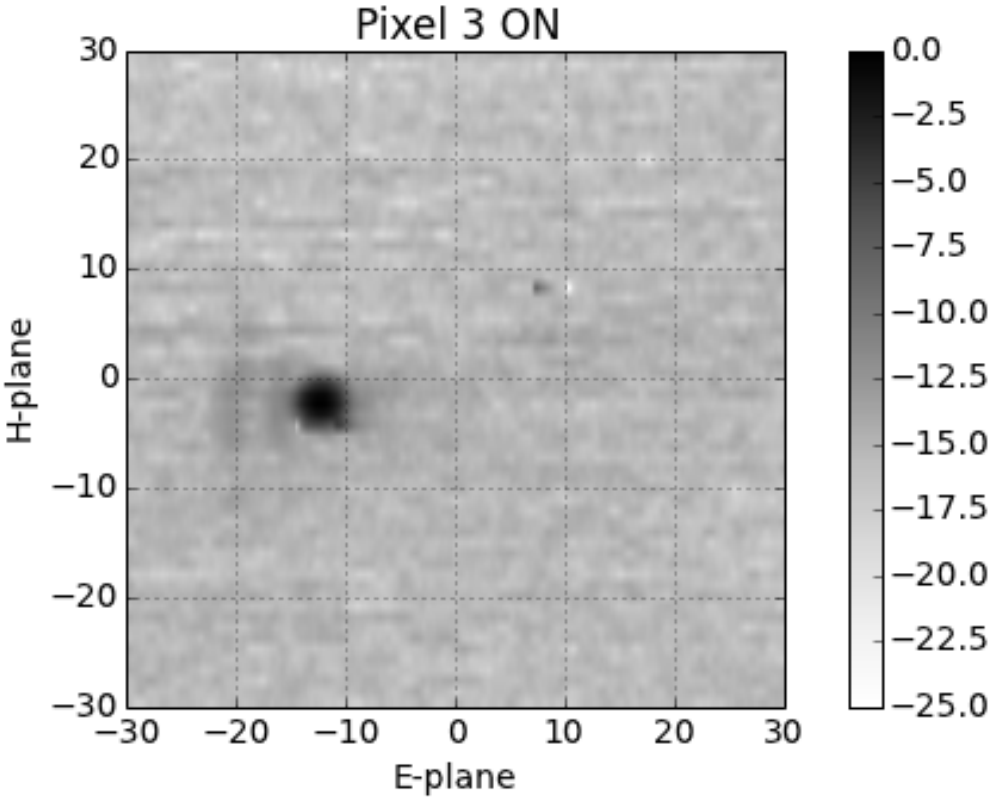
Measured Antenna Patterns



- Pattern depend on the secondary antenna
- Other lenses can be used to fit application requirements
- Side lobes are 15dB down

- Loaded source configurations for 16, 7, 4, and 1pixel
- Power down switching time is 0.5ns
- 16 beams cover a ±15º field-of-view

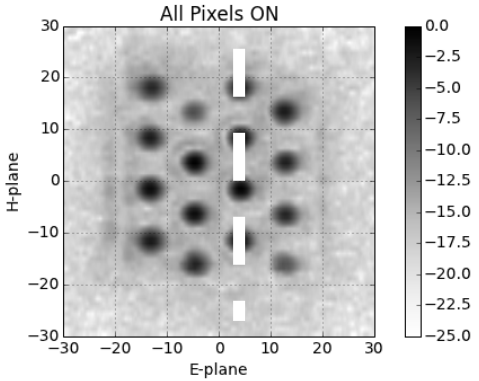
Measured Antenna Patterns

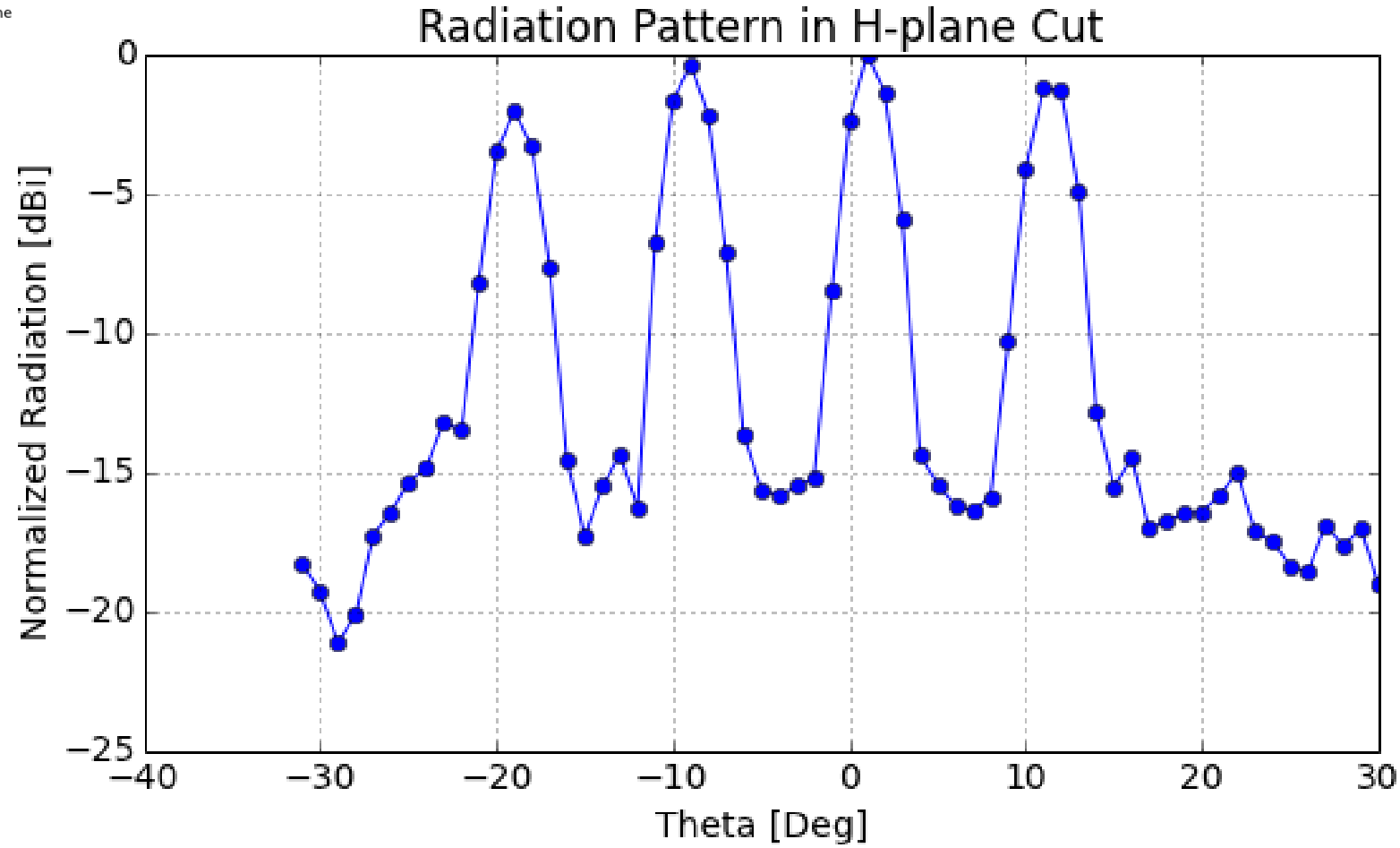


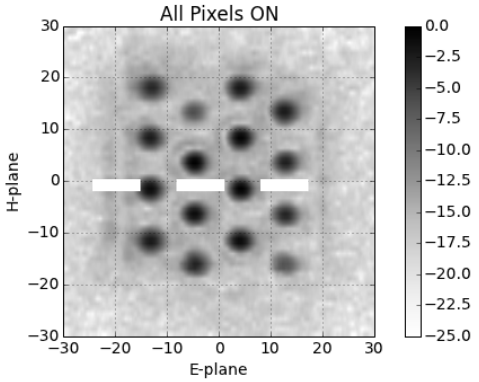
- Pattern depend on the secondary antenna
- Other lenses can be used to fit application requirements
- Side lobes are 15dB down

- Loaded source configurations for 16, 7, 4, and 1pixel
- Power down switching time is 0.5ns
- 16 beams cover a ±15º field-of-view

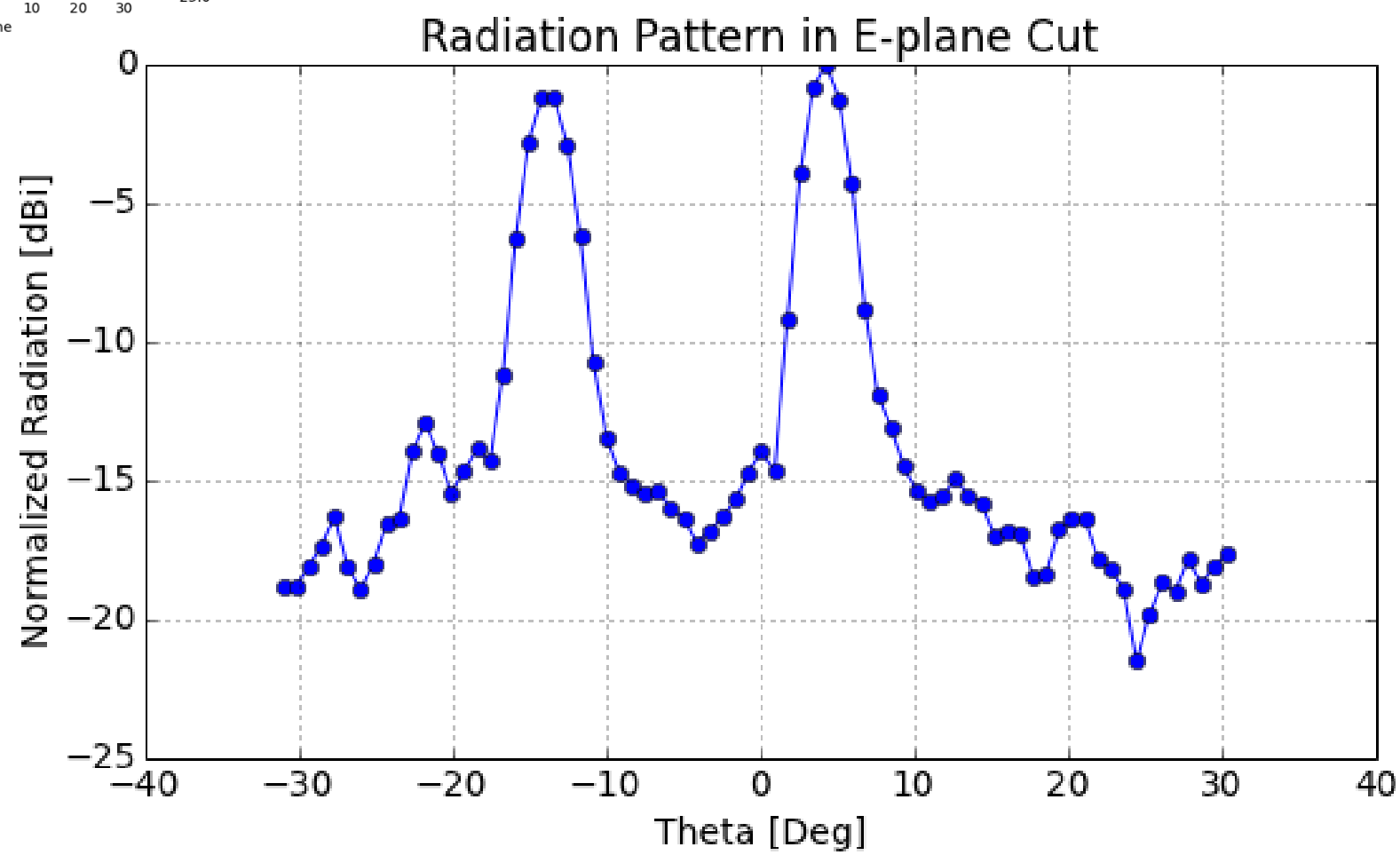
H-plane Cut



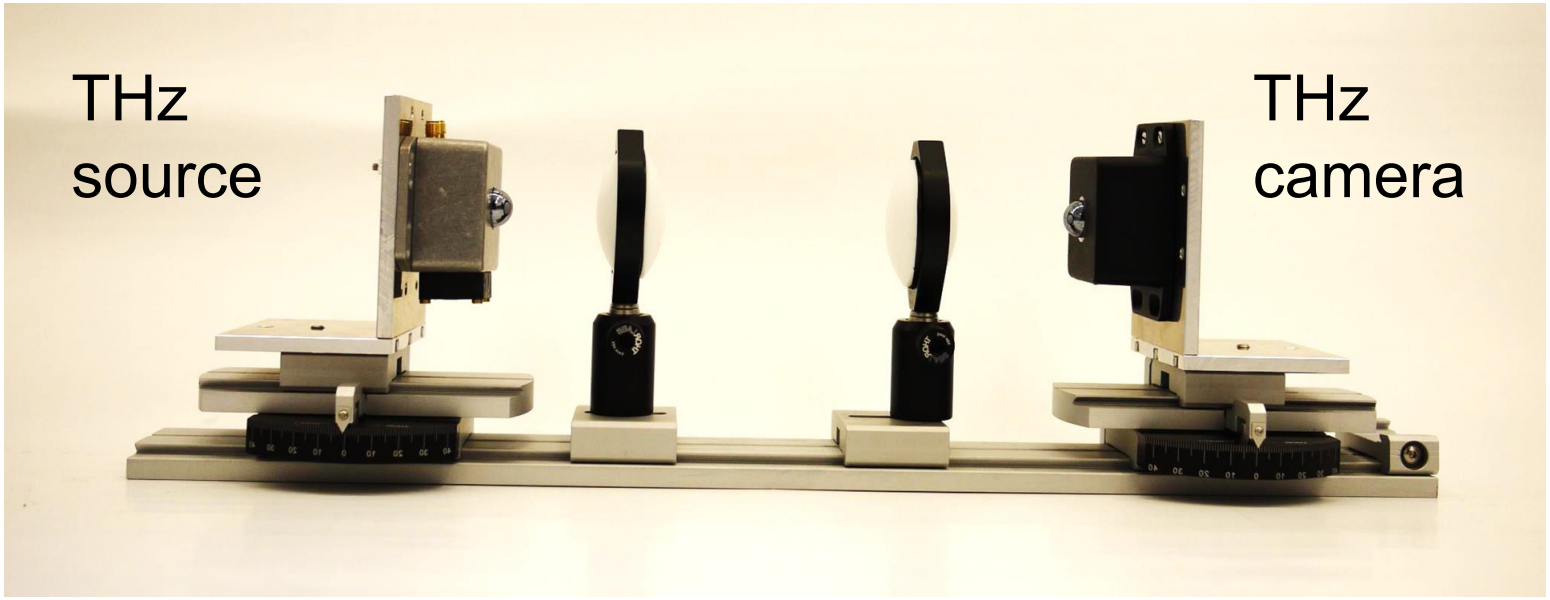




E-plane Cut



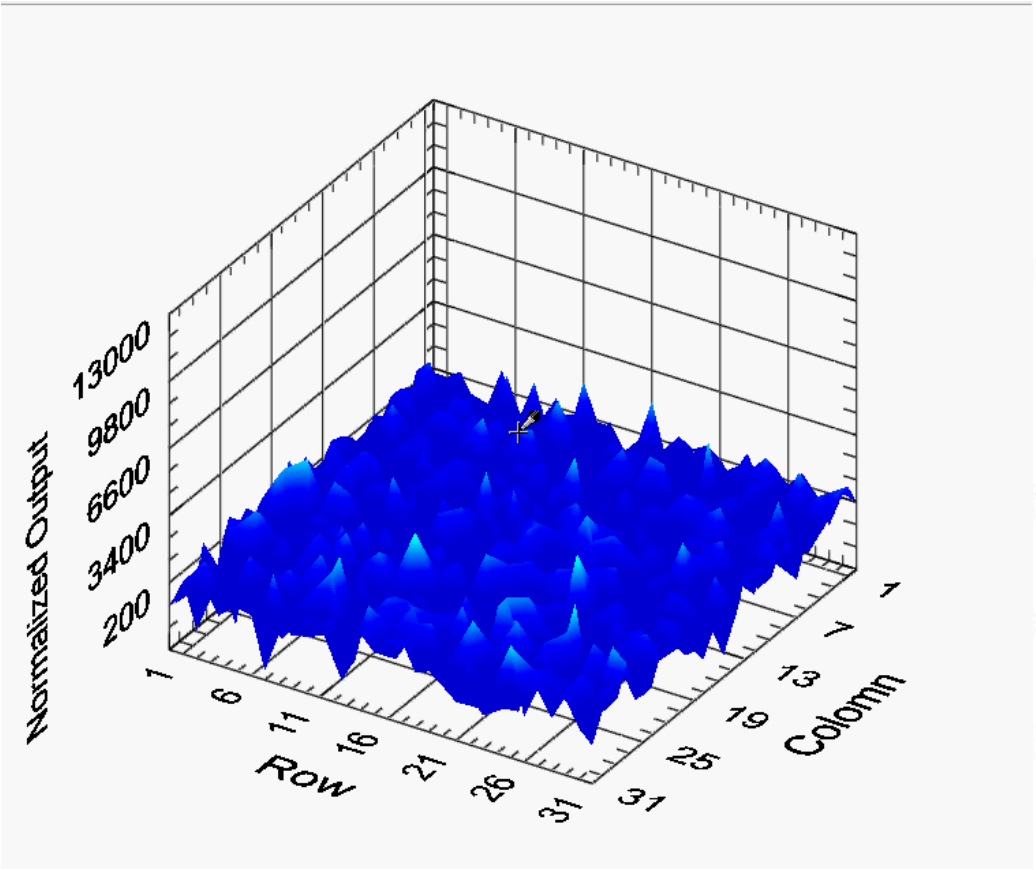
THz Imaging Demonstration



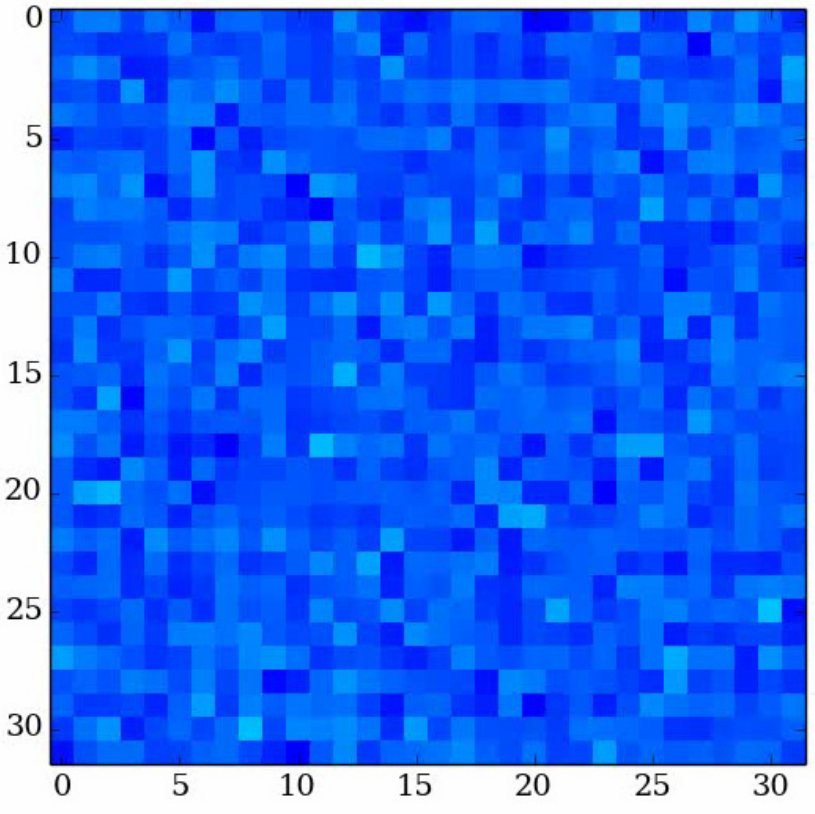
- The source array illuminates a 1k-pixel CMOS terahertz camera module [ISSCC12]
- Arbitrary pattern can be loaded into the source via USB to achieve a uniform background illumination
- The real-time stream of the CMOS camera is displayed on the computer screen with 25fps
- Was shown on Monday's demonstration session

Recorded Illumination

Single beams



Diffused background



Summary

Tech.	Freq.	Radiated Power	EIRP	Pixel	BW	DC-to-RF Eff.	Area	Ref.
	[GHz]	[dBm]	[dBm]		[%]	[‰]	[mm^2]	
65nm bulk	260	0.5	15.7	8	9.5	1.4	2.3	[3]
45nm SOI	280	-7.1	9.4	16	3.2	-	7.3	[4]
65nm bulk	288	-4.1	14.2	1	0.7	1.4	0.29	[5]
45nm bulk	553	-36.5	-	1	-	3.4E-4	0.29	[6]
250nm SiGe	825	-29	-17	4	1.8	2.7E-4	3.22	[7]
130nm SiGe	519 to 536	0 (all) -12 (single)	25	16	3.2	0.4	4.2	This Work

Conclusions

- Highest radiated output power for a single CW source above 500GHz (-12dBm, 25dBm EIRP)
- Highest total radiated power from a single silicon chip above 300GHz (0dBm)
- Provides diffuse THz illumination with programmable diversity (reconfigurable)
- Low-cost chip-on-board packaging, no waveguide integration required
- Radiation can be recorded with a CMOS 1k-pixel camera – an all Si THz imaging solution

Acknowledgements

- This work was supported in part by the European Science Foundation through a European Young Investigator Award.
- Thanks goes to Hans Keller, University of Wuppertal, for his support.

A Scalable Terahertz 2D Phased Array with +17dBm of EIRP at 338GHz in 65nm Bulk CMOS

Yahya Tousi

Ehsan Afshari

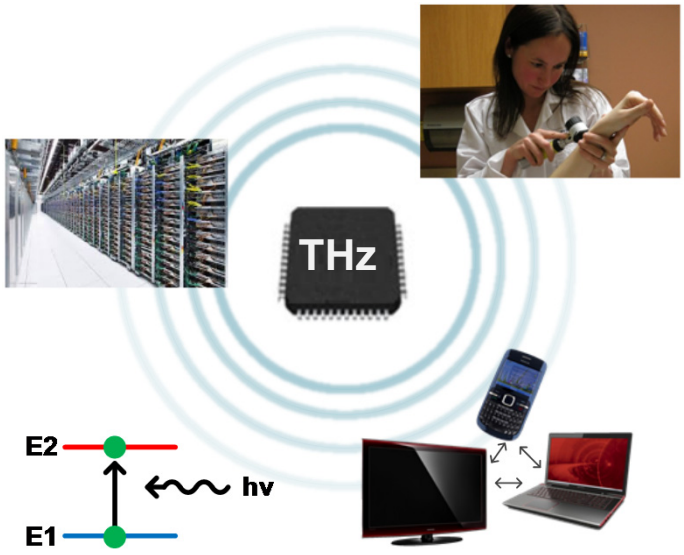
Cornell University

Outline

- Introduction
- Theory of coupled oscillatory networks
- A 2D scalable terahertz phased array
- Circuit design and implementation
- Prototype measurement
- Conclusion

Integrated Terahertz

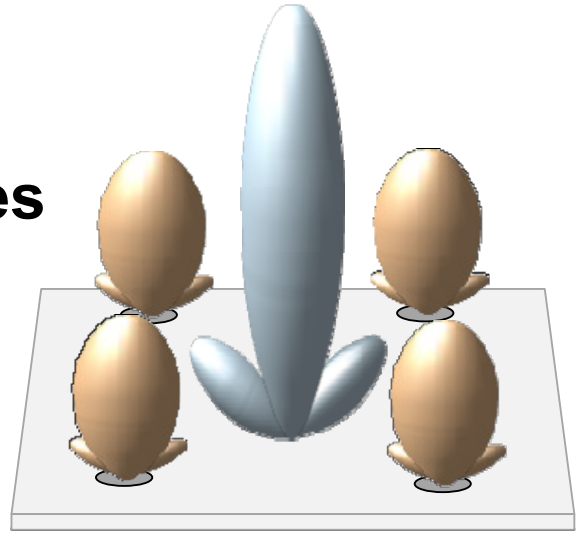
- Why explore terahertz integration on CMOS?
  - Make numerous potential applications practical
- Deliver low-cost applications in:
  - Non-invasive medical imaging
  - Stand-off imaging and sensing
  - Ultra-wide band communication
  - Particle spectroscopy



Integration: Challenges and Opportunities

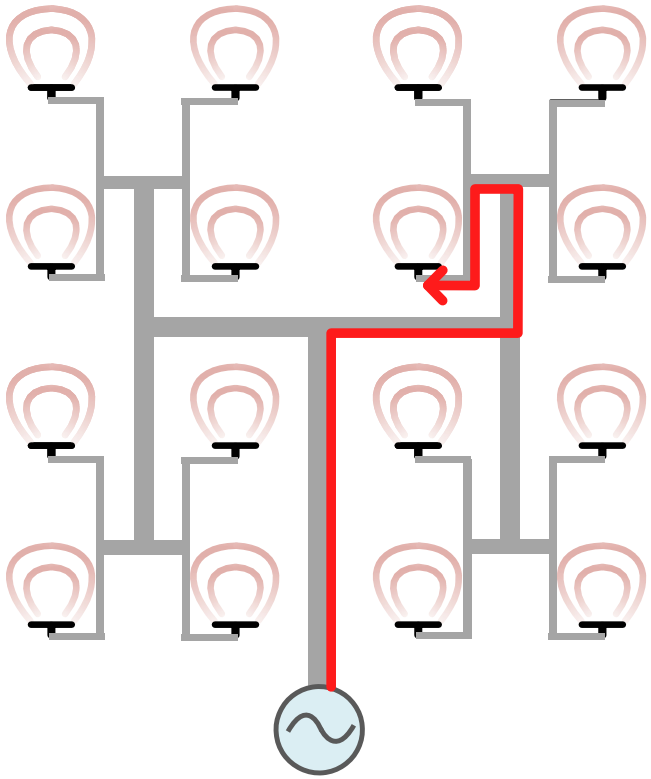
- **Challenges**:
  - **At the limits of transistors:** $\mu_{Si} \overset{\text{yields}}{\Longrightarrow} f_{max} \overset{\text{yields}}{\Longrightarrow} P_{available}$
  - **Limited available power of individual devices**
- **Opportunities**:
  - **Collective arrays of multiple devices**
  - **Integrated radiation**

$$EIRP_{array} = N^2 \times P_{available}$$



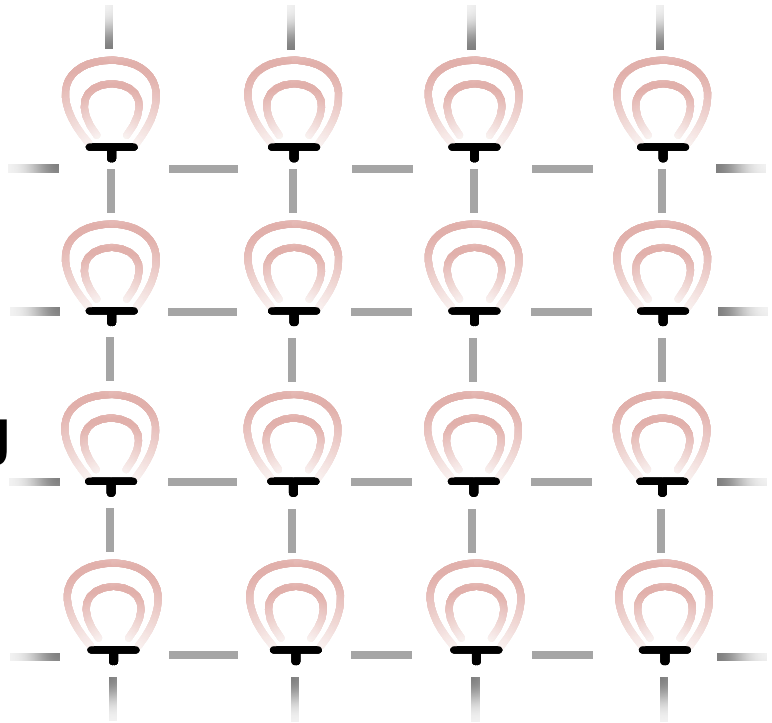
Why is Scalability Crucial at Terahertz?

- **To achieve collective performance:**
- **Systematic use of many devices**
- **Avoid long signal propagation**
- **Issues of regular phased arrays:**
- **Controlled from a central node**
- **Challenging to scale**
- **Propagation of error and loss**



The Coupling Perspective

- Concept: distributed sources of radiations
- Advantages:
  - Fully distributed
  - Spatial power combing
  - Nearest neighbor coupling
  - Symmetric dynamics
  - Error distribution



Distributed Dynamics

- This is the way many large scale phenomena occur in nature.
- Collective dynamics of a network of coupled elements
- <u>Examples</u>:
  - Nature: flocking patterns
  - Physics: phase transitions
  - Computation: distributed processors

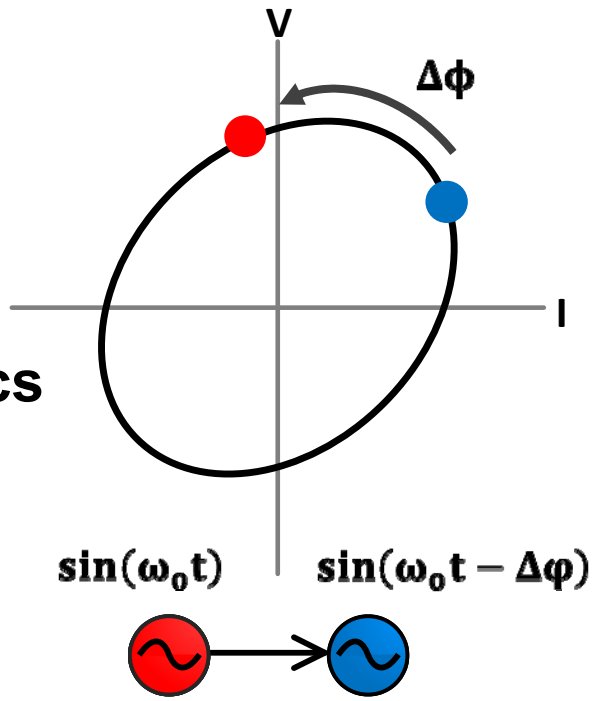
<u>Distributed dynamics for a synchronized phased array</u>

Outline

- Introduction
- Theory of coupled oscillatory networks
- A 2D scalable terahertz phased array
- Circuit design and implementation
- Prototype measurement
- Conclusion

Theory of Coupled Oscillators

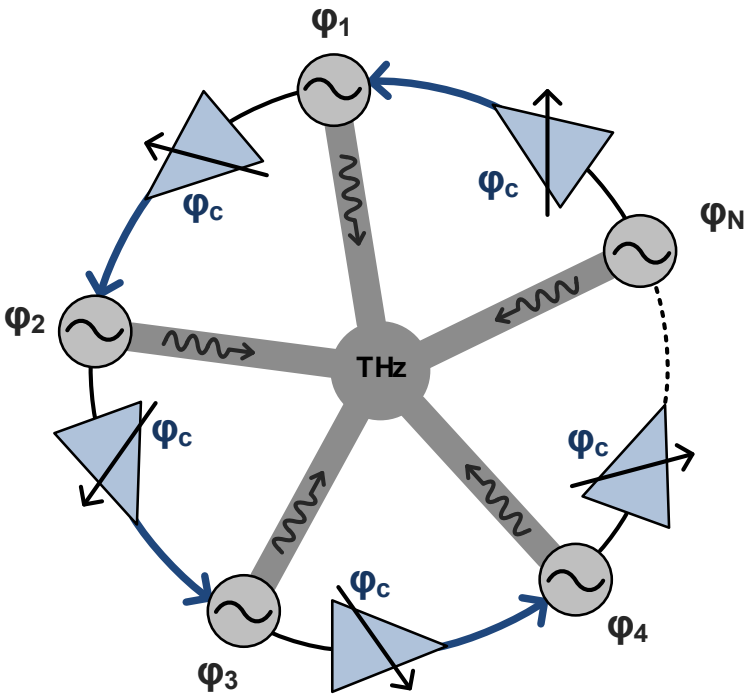
- **Adler's model for coupling:**
  - **Models only the phase evolution**
  - **Coupling alters the oscillator dynamics**
- **Examples of electrical coupling**
  - **Injection locking dividers**
  - **Quadrature oscillators**
  - **Delay-coupled oscillators (DCO) for frequency tuning**



$$\Delta\Phi = \sin^{-1}\left(\frac{\Delta\omega}{\omega}\cdot 2Q\frac{V_{core}}{V_{inj}}\right)$$

Delay Coupled Oscillators

- DCO*: A distributed synchronized source
- *N* delay coupled oscillators
- <u>Advantages of DCO:</u>
  - ➢ High power, tunable THz source
  - ➢ Decouples tuning form the core
  - ➢ Efficient power combining
  - ➢ Tunable to many modes

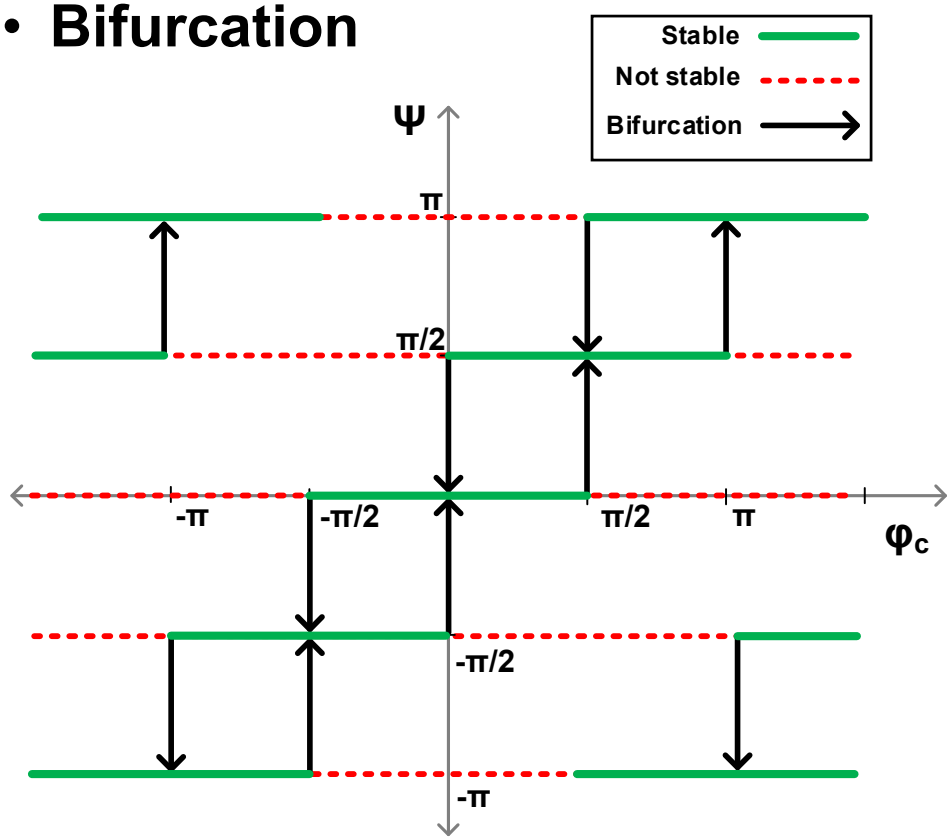


$$\Delta\omega = \sin\left(\phi_{inj} + \phi_c - \phi_{core}\right) \cdot \frac{\omega_o}{2Q} \frac{V_{inj}}{V_{core}}$$

* Tousi, et al., ISSCC 2012

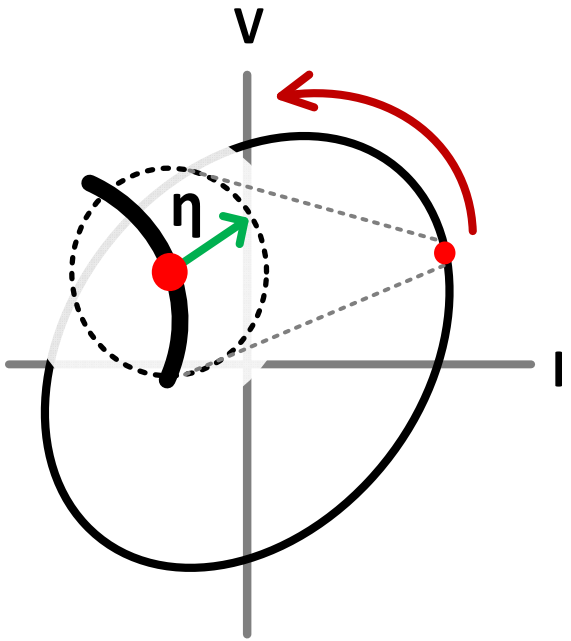
Stable Coupling Modes (N=4)

- Dynamical Analysis
  - Stable modes
  - Bifurcation



Stability Criteria:

$$\Lambda\left(\frac{\dot{\eta}}{\eta}\right) < 0$$



Scalable Coupled Oscillators

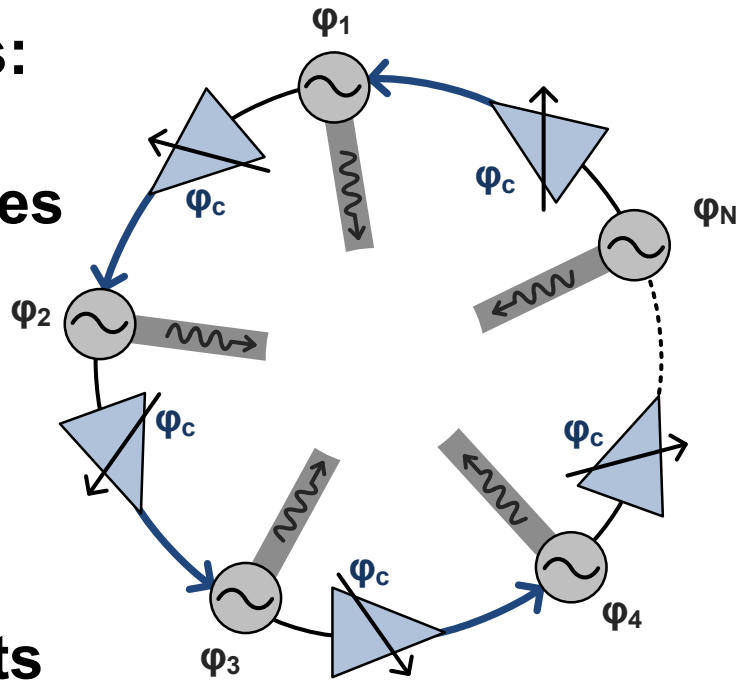
- How can we scale this structure?
- A network of scalable radiators:

✓ 2D scalable dynamical properties

✓ Symmetric dynamics

✓ Based on local connections

✓ Control over individual elements

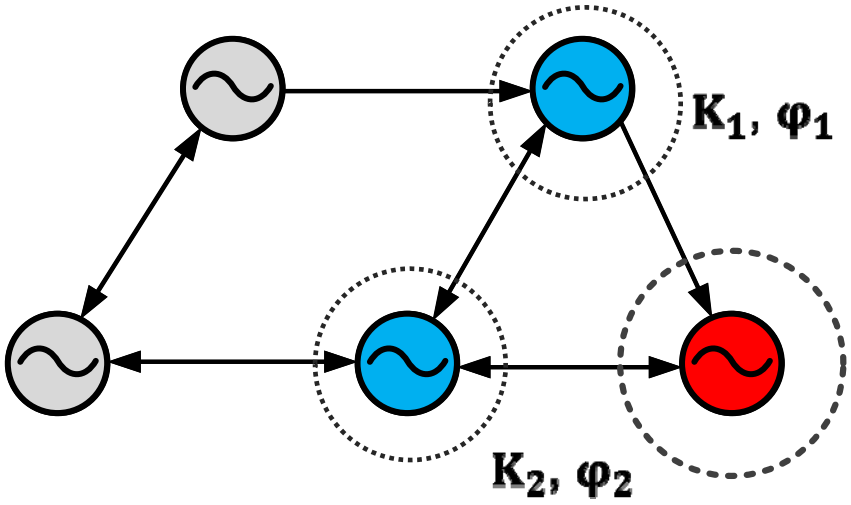


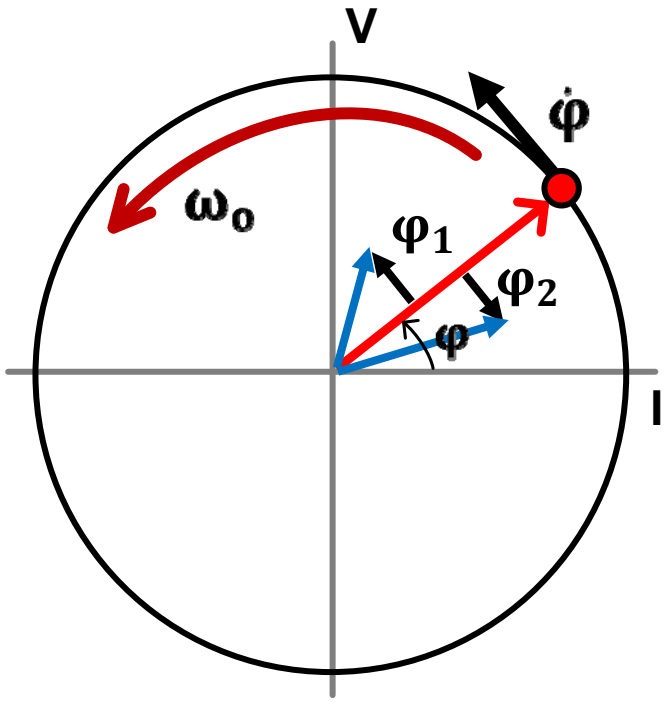
Outline

- Introduction
- Theory of coupled oscillatory networks
- A 2D scalable terahertz phased array
- Circuit design and implementation
- Prototype measurement
- Conclusion

Generalized Adler's Equation

- An arbitrary arrangement of coupled cores



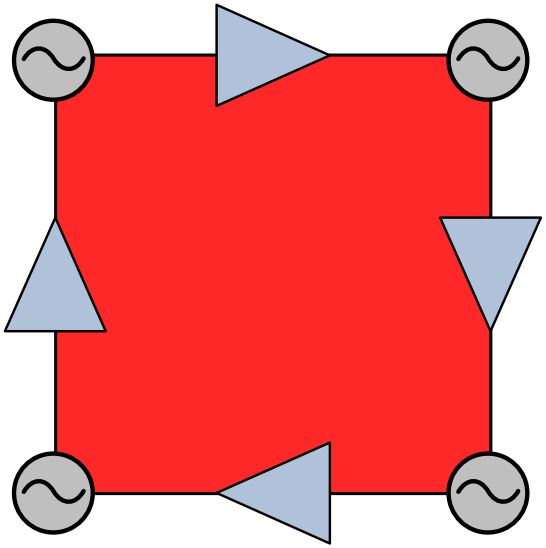


Generalized Adler's Equation

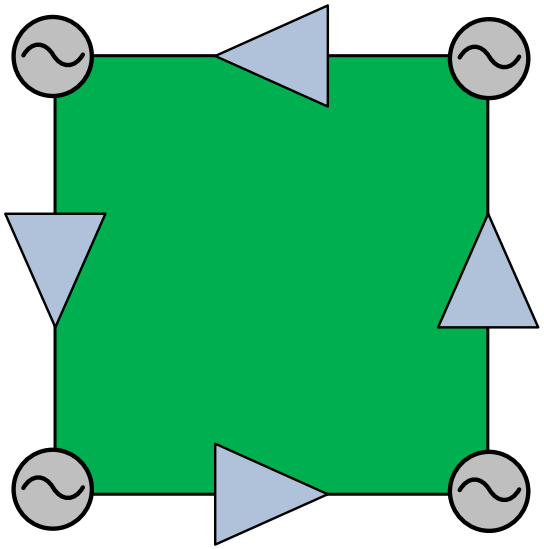
$$\dot{\varphi} = \omega_o + K_1 \sin\varphi_1 + K_2 \sin\varphi_2 + \cdots$$

Delay Coupled Phased Array

- **Tiling: To produce repeatable patterns of coupled oscillators in 2D**



Tile 1: Clockwise Loop

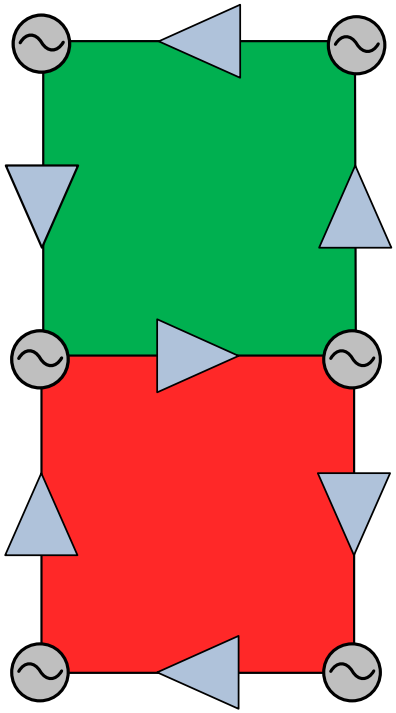


Tile 2: Counter Clockwise Loop

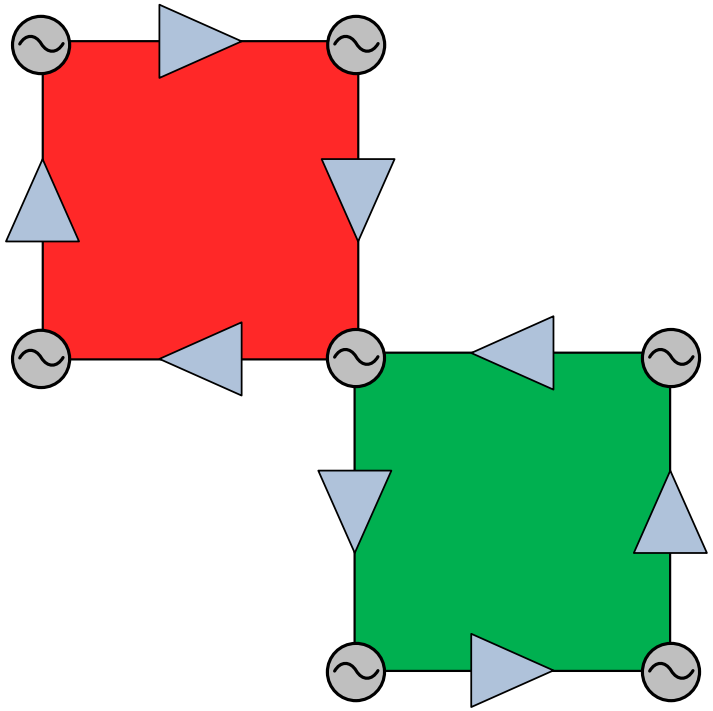
Construction of the Lattice

- Two ways to construct the lattice

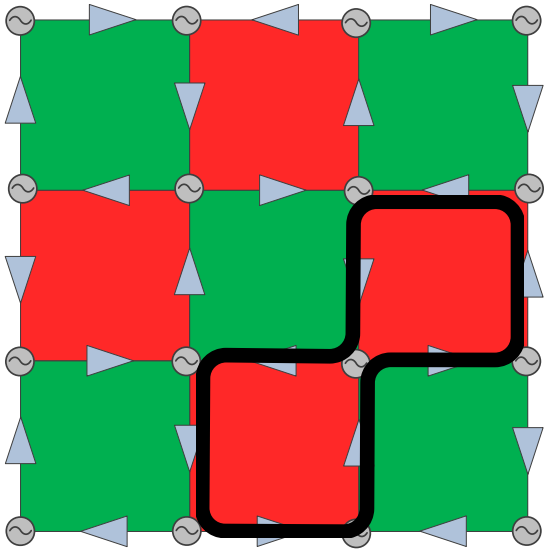
(a) Edge-to-Edge



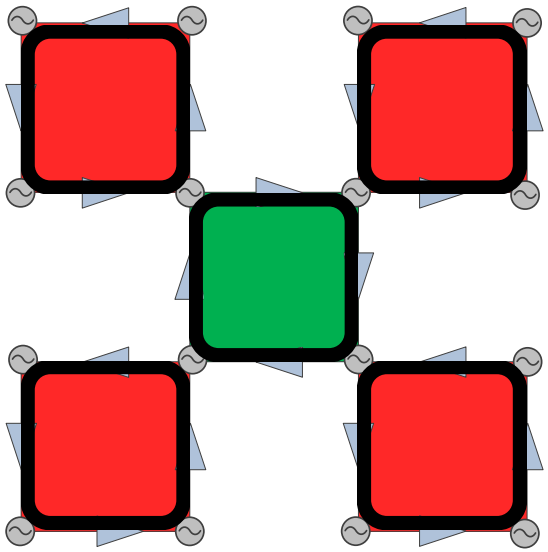
(b) Vertex-to-Vertex



Possible Rectangular Array Patterns



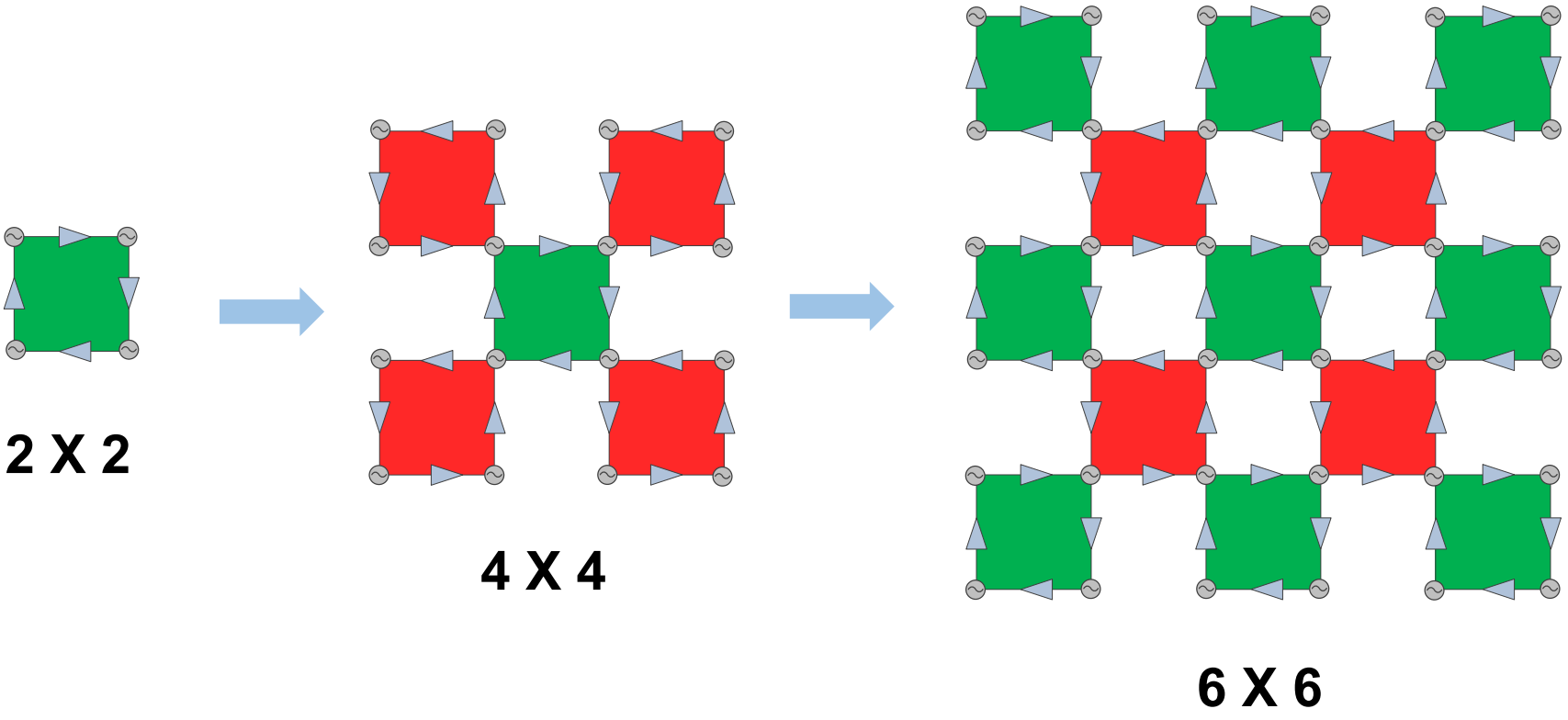
(a) Edge-to-Edge



(b) Vertex-to-Vertex

Scaling to Higher Dimensions

- **Scaling the coupled network**



Symmetric Dynamics

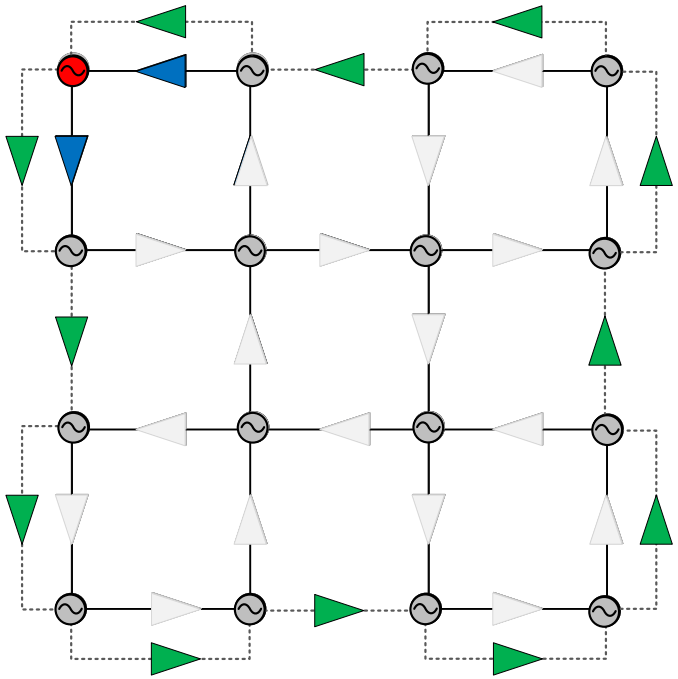
- **How to address difference between the central nodes and the edges?**

Center nodes:

$$\dot{\varphi} = \omega_o + K \sin\varphi_1 + K \sin\varphi_2$$

Grid boundaries:

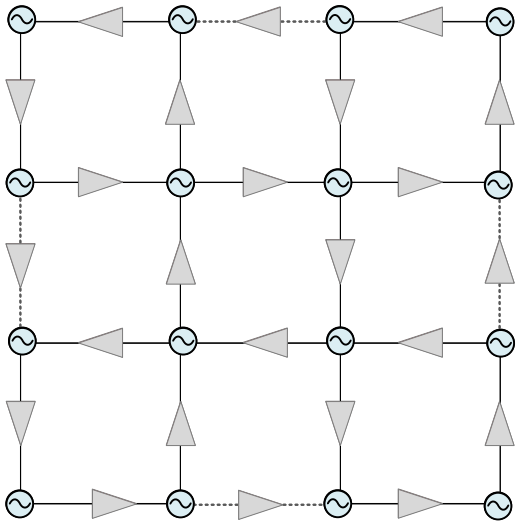
$$\dot{\varphi} = \omega_o + K \sin\varphi_1 + K \sin\varphi_2$$

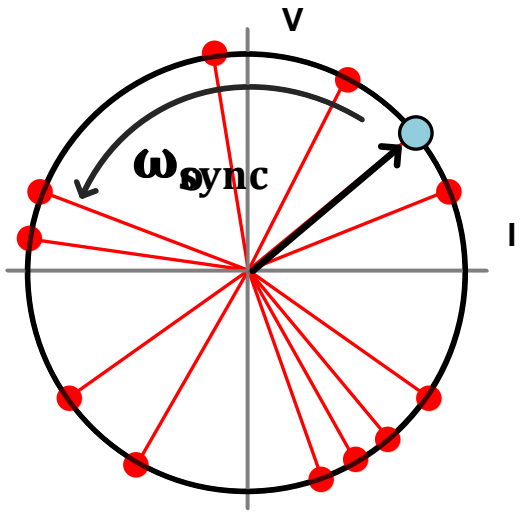


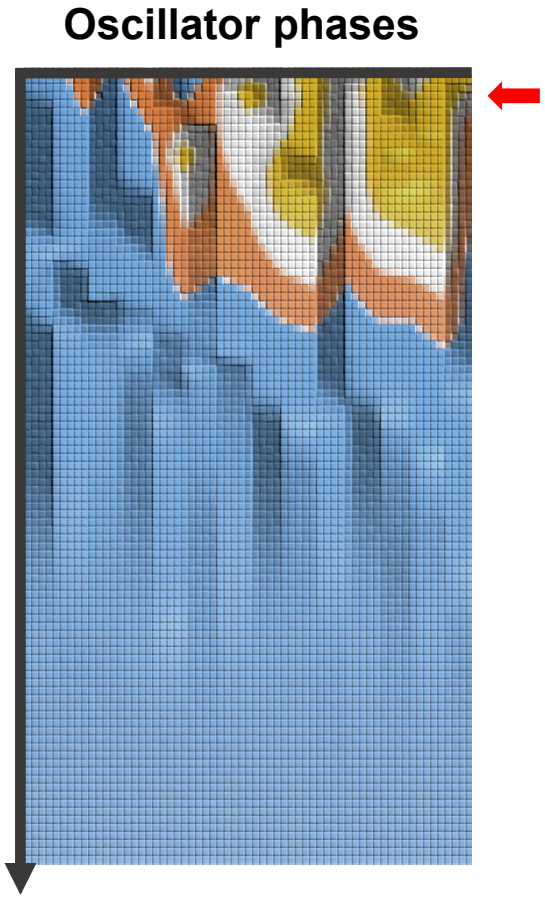
- **The same dynamic is systematically replicated across the entire grid**

Synchronization

- Synchronization from initial condition.





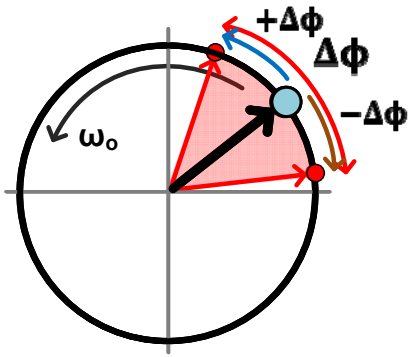


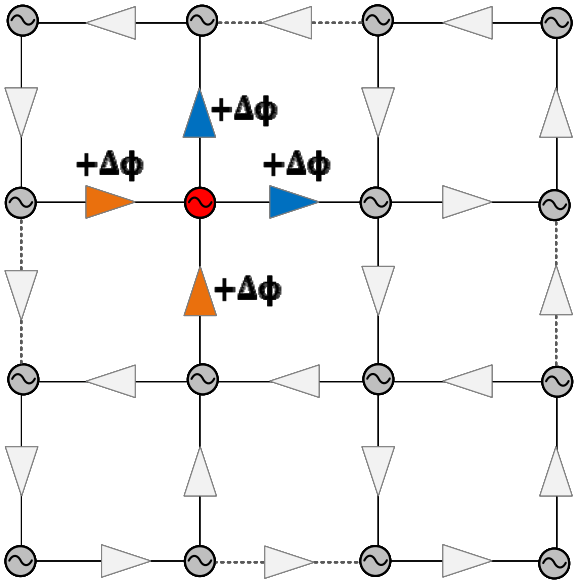
- All cores synchronize in-phase

Selective Phase Control

- Individual phase-tuning of core oscillators
- Tuning each core without disturbing others

$$\omega_{sync} = \omega_o + \sum_i K \sin \varphi_i$$



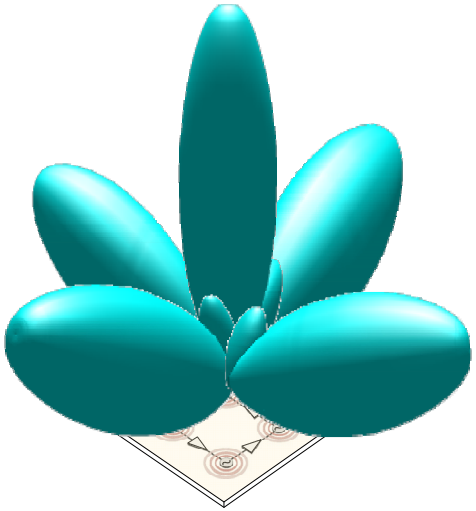


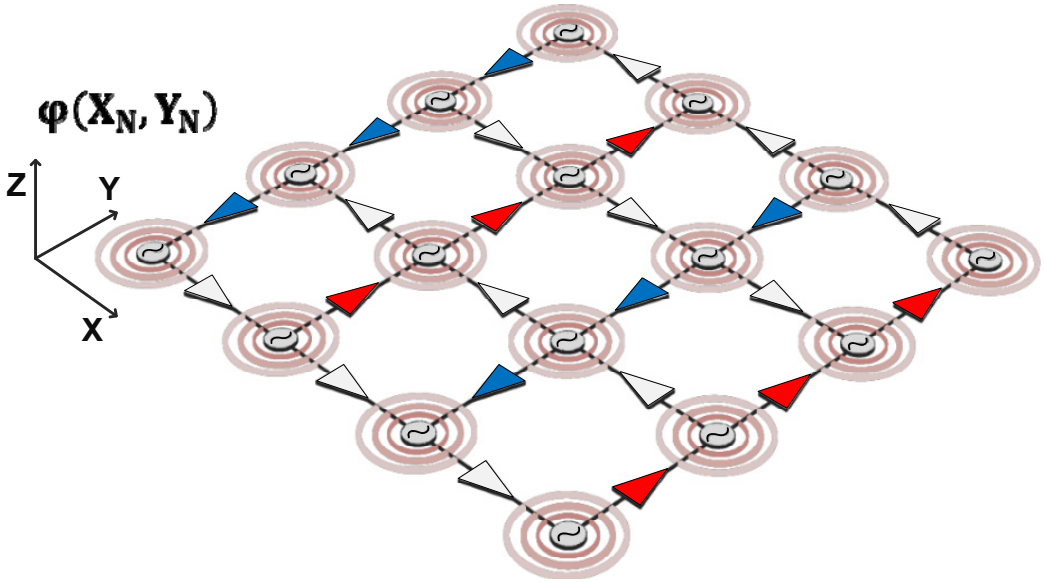
➡ $\varphi_{core} = \varphi_{prior} + \varphi_{coupler}$

➡ $\varphi_{core} = \varphi_{next} - \varphi_{coupler}$

Beam Steering Technique

- Phase tuning of the array in both angles
- 2D beam forming in the front lobe

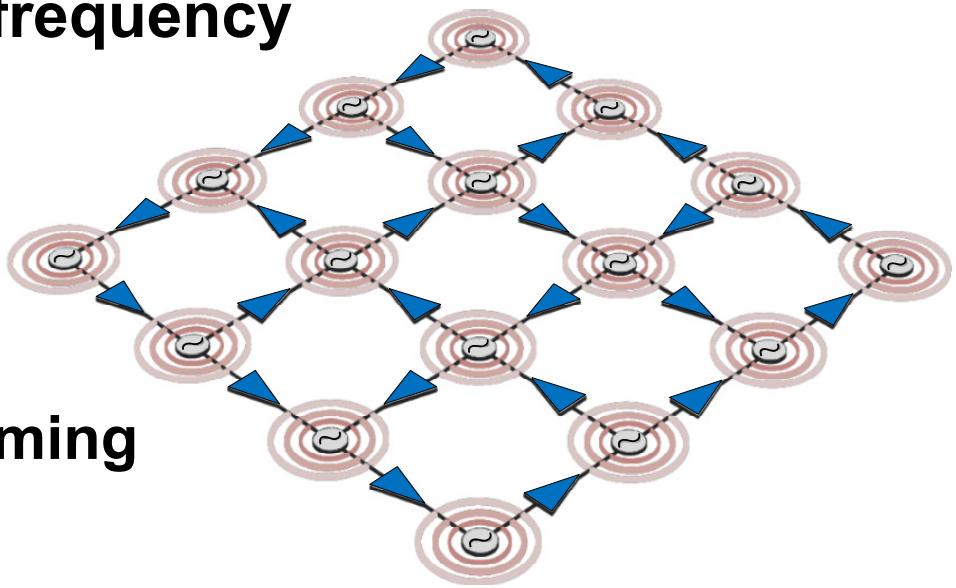




$$\varphi(X_{N+1}Y_NY_M) = \varphi(X_N, Y_N) + \Delta\varphi$$

Tuning the Synchronized Frequency

- What if we change all couplers together?
- Tuning the synchronized frequency
- Frequency/beam control



- **Differential**:

✓ Phase profile → Beam forming

- **Common**:

✓ Frequency tuning

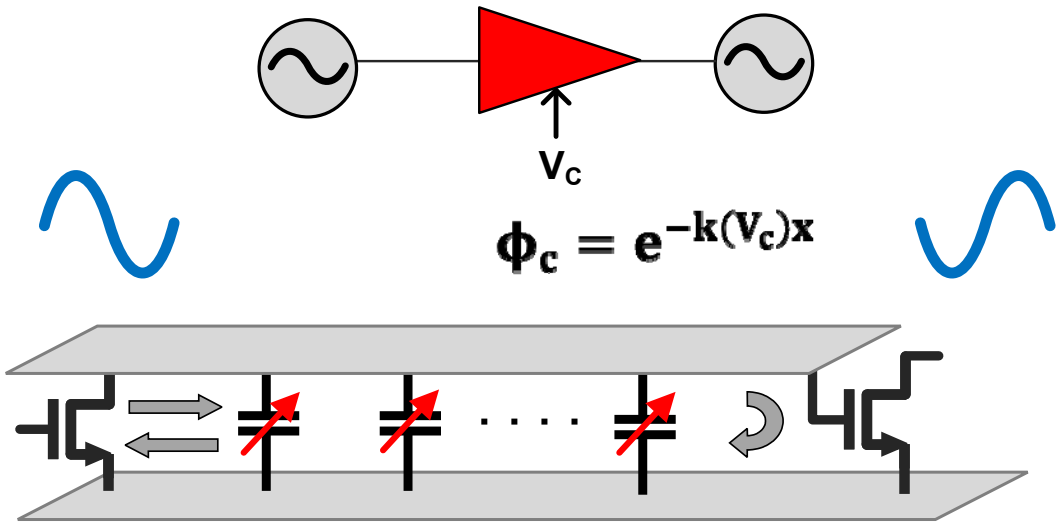
$$\omega_{sync} = \omega_o + \sum_i K \sin \varphi_i$$

Outline

- Introduction
- Theory of coupled oscillatory networks
- A 2D scalable terahertz phased array
- Circuit design and implementation
- Prototype measurement
- Conclusion

Distributed Phase Shifters

- Concept: progressive phase shift in multiple stages
  - Absorbs the interconnections
  - Wide bandwidth
  - Low profile
- Phase shifter
  - Matched input
  - Reflective output



The Oscillator

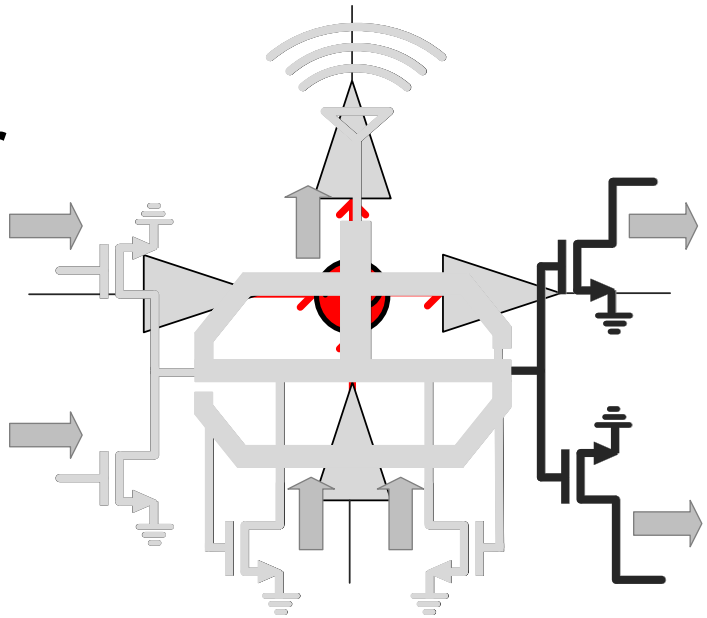
- Core oscillator and coupling interface

➢ Core oscillator

  - Maximize the harmonic power
  - Deliver the power to antenna

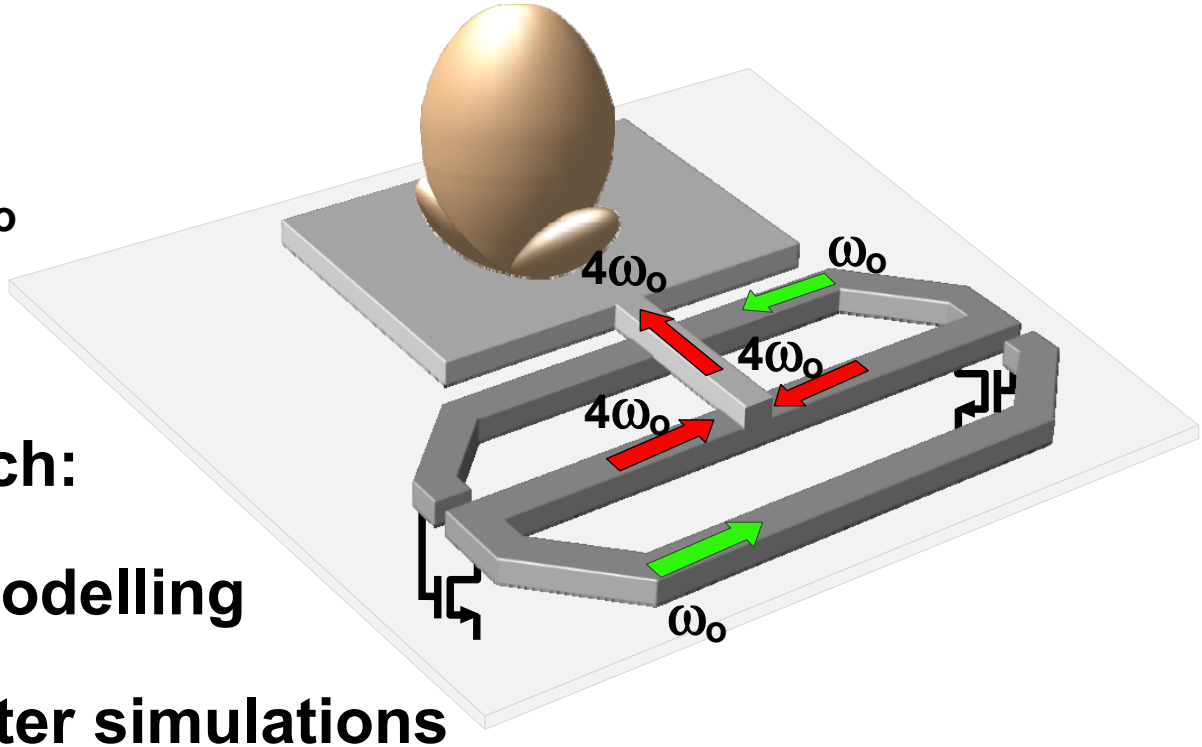
➢ Connection to neighbors

  - Receive input coupling
  - Inject energy to outgoing couplers



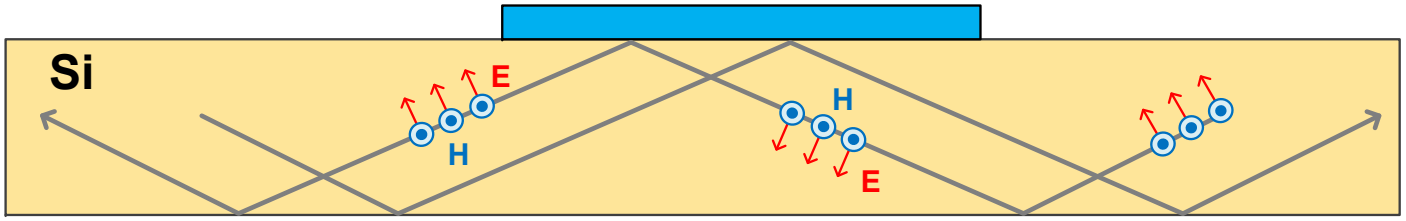
Core Oscillator Design

- Core transistors and the distributed passive network
- Responsibilities:
  - Resonance at ω_o
  - Matching at $4\omega_o$
- Modelling approach:
  - HFSS passive modelling
  - 5-port S-parameter simulations



Fully Integrated Antenna

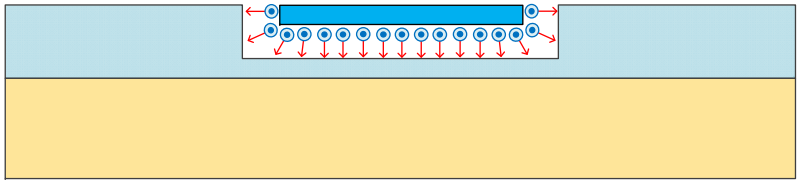
- Challenges of radiation on silicon:
  - Substrate coupling
  - Costly to compensate



Double sided

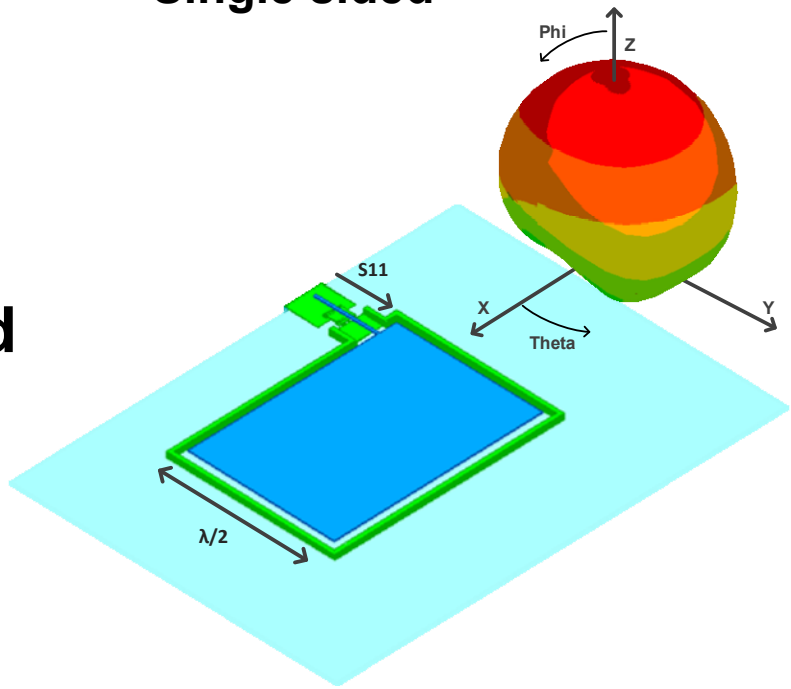
Fully Integrated Antenna

- Challenges of radiation on silicon
  - Substrate coupling
  - Costly to compensate



Single sided

- Patch antenna:
  - \+ Lens-less antenna
  - \+ No wafer thinning is needed
  - − Lower bandwidth



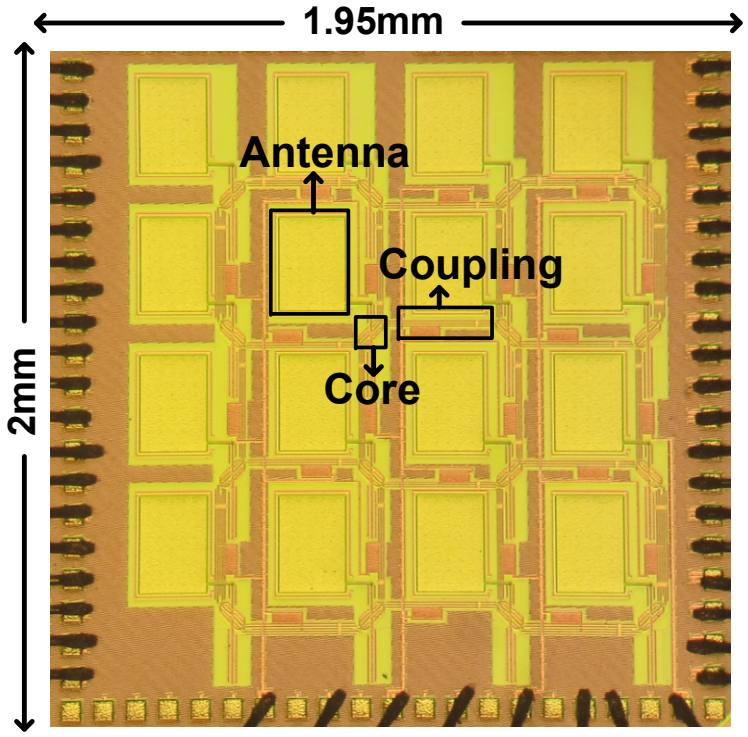
- Radiation efficiency

Outline

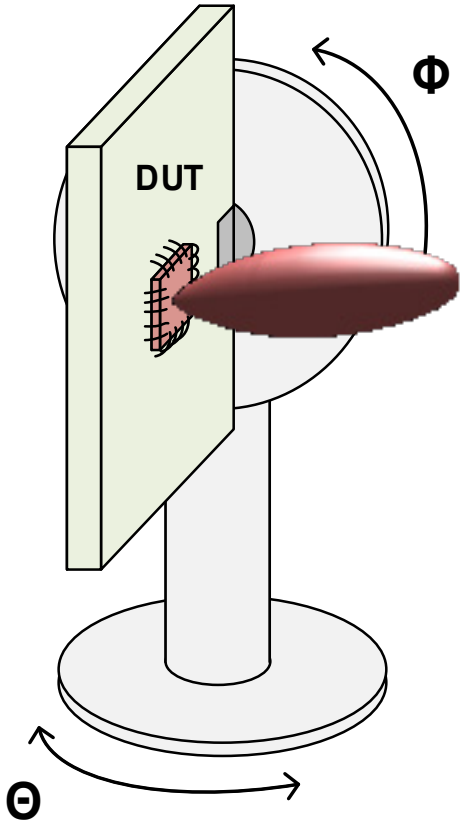
- Introduction
- Theory of coupled oscillatory networks
- A 2D scalable terahertz phased array
- Circuit design and implementation
- Prototype measurement
- Conclusion

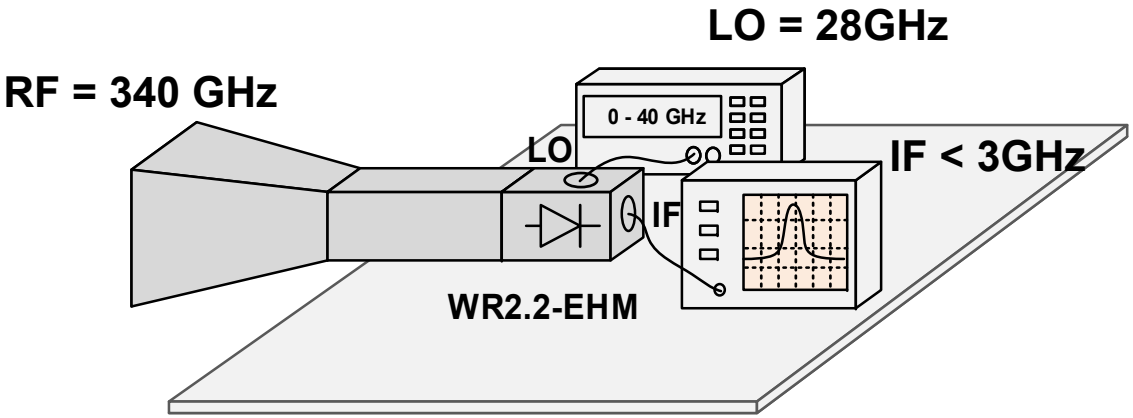
Terahertz Phased Array

- Technology: 65nm bulk CMOS process
- Array dimensions: 4 rows and 4 columns
- Center frequency: 340 GHz
- Spatial beam forming
- Lens-less radiation
- No post processing



Spectrum Measurement

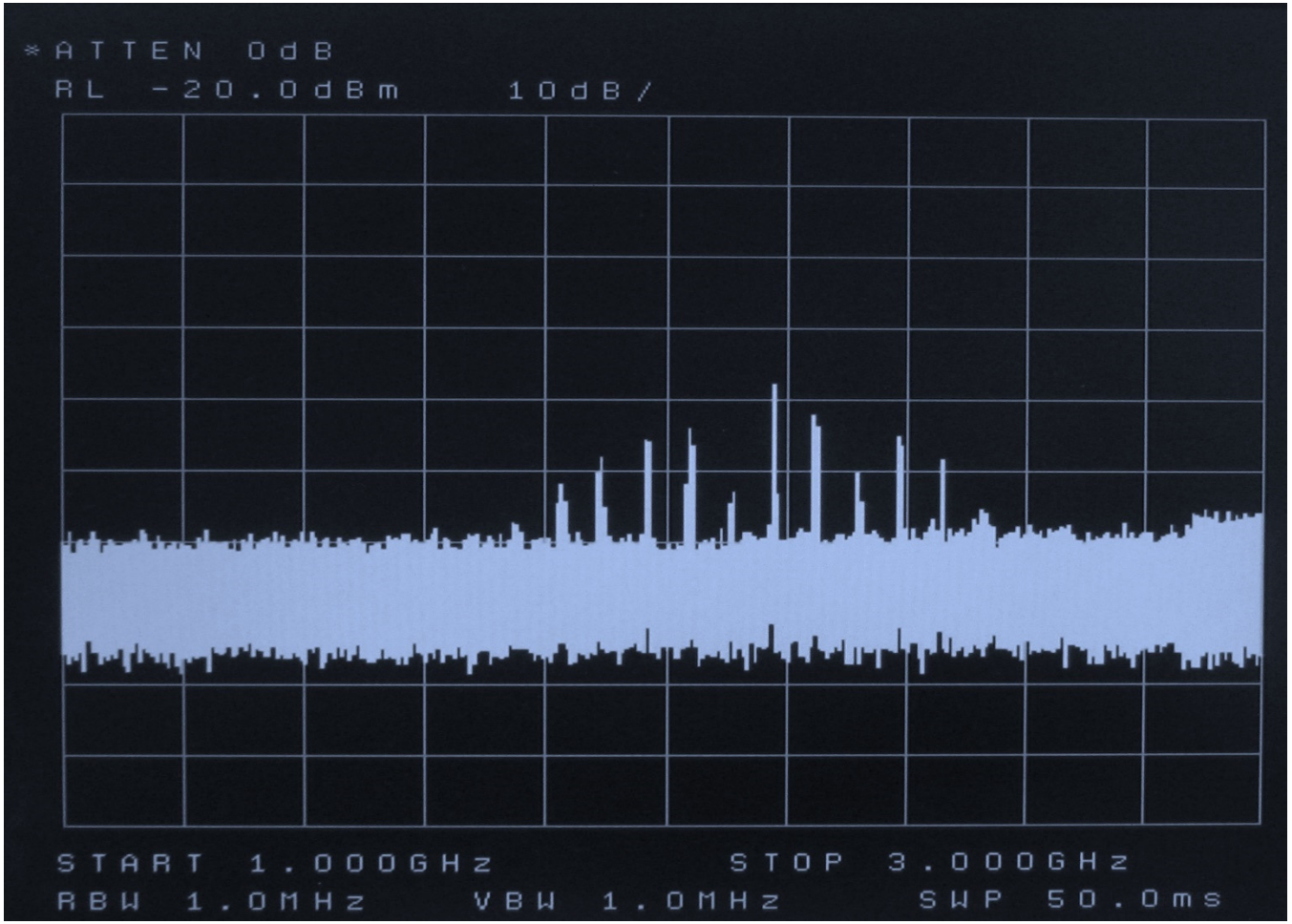




- **Observing core synchronization**
- **Frequency**
- **Phase noise**

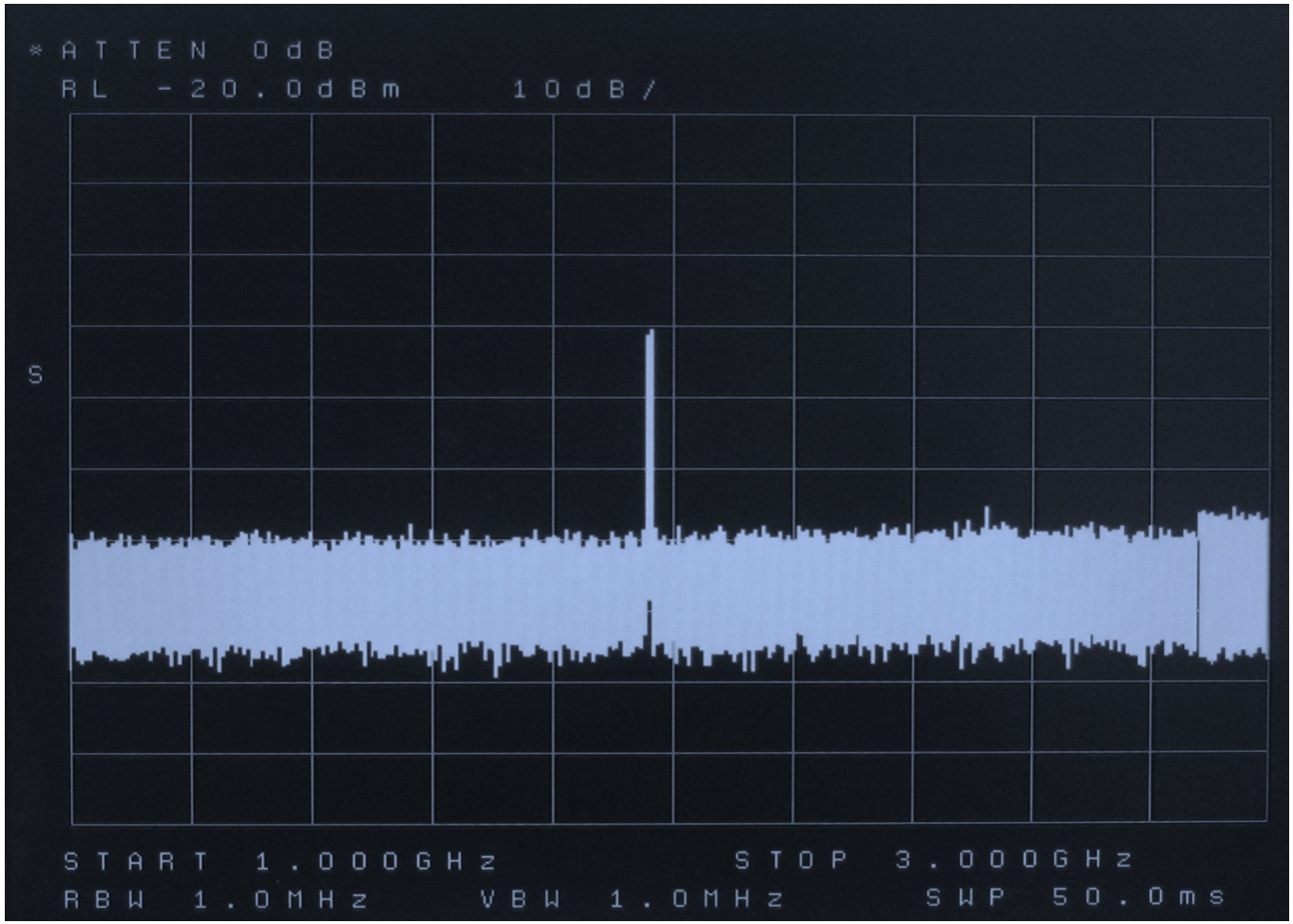
Synchronization

Coupling:
Off

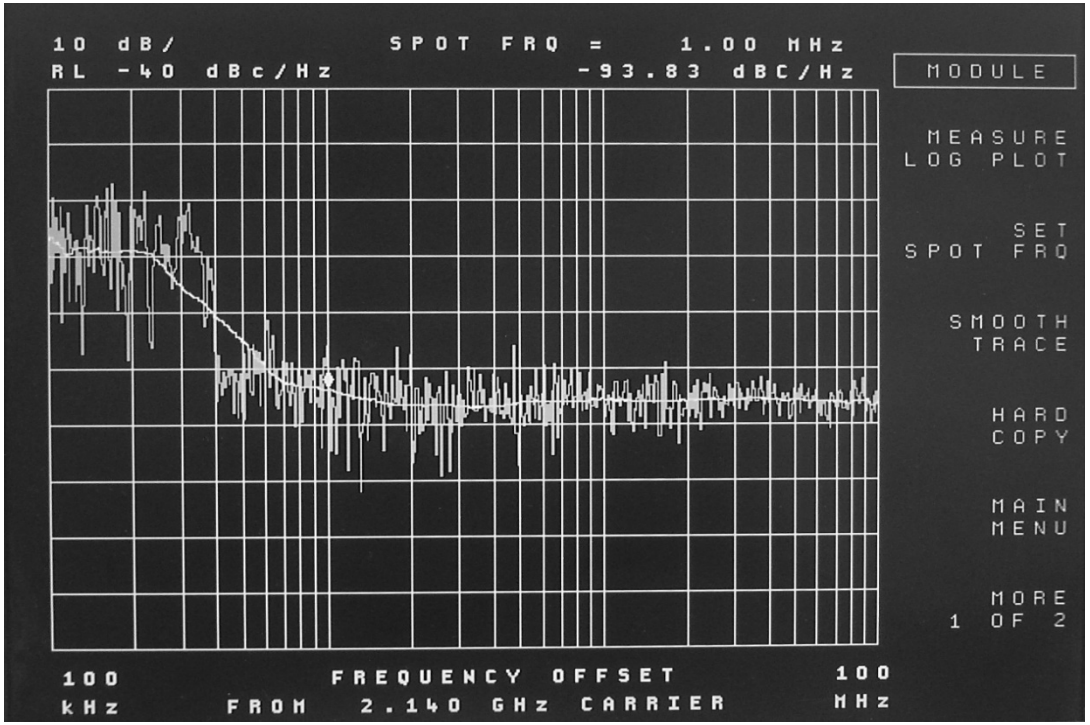


Synchronization

Coupling:
On



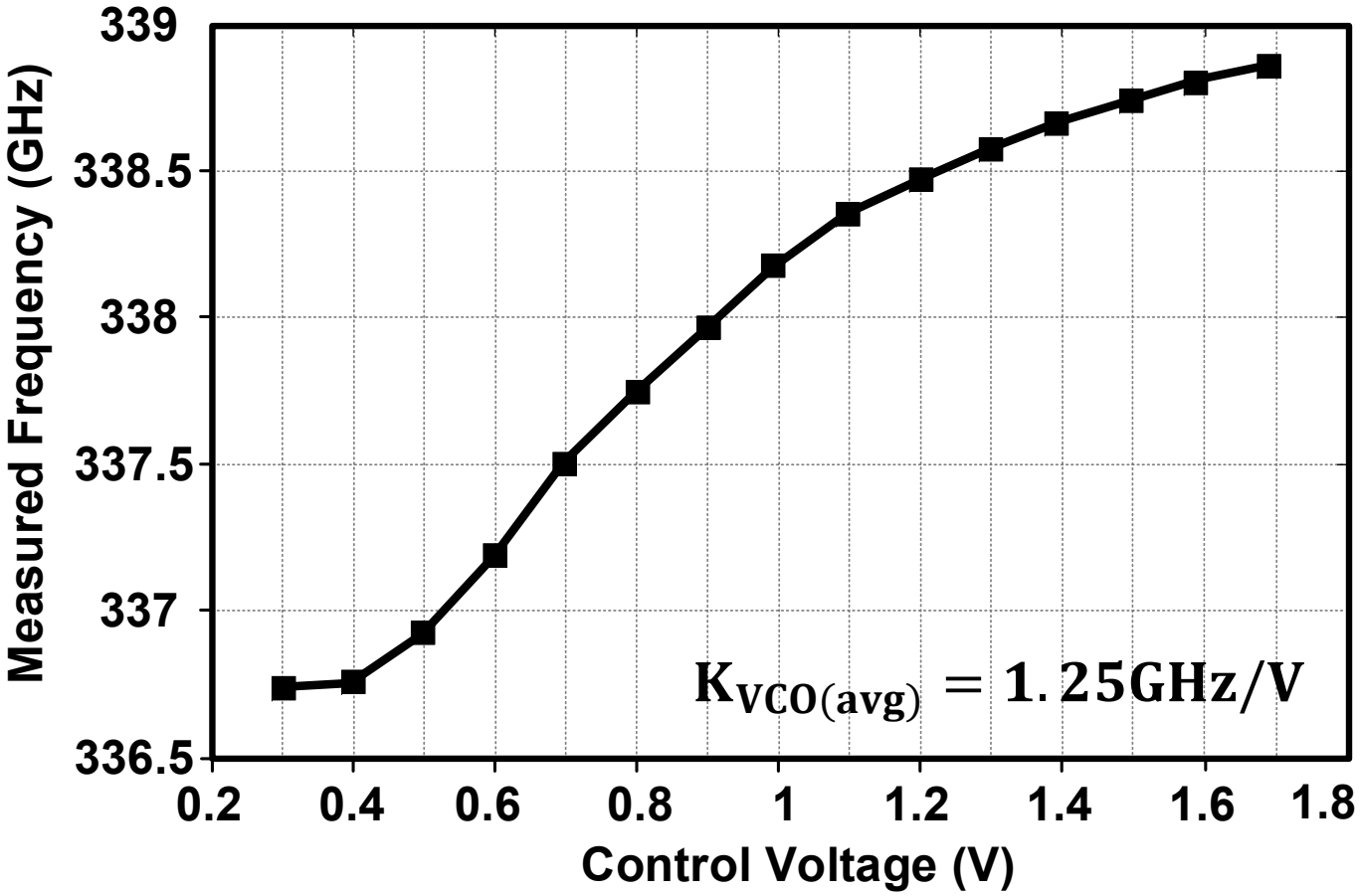
Phase Noise



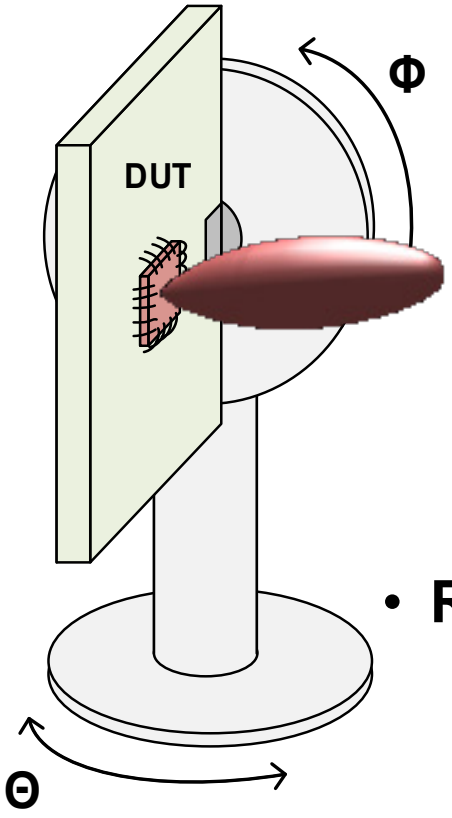
- **Measured at 338GHz: -93dBc/Hz @ 1MHz offset**
- **Best phase noise on silicon above 100GHz**

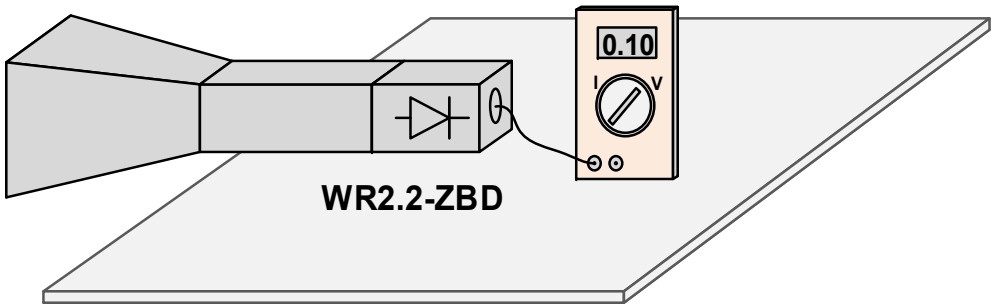
Frequency vs. Control Voltage

- **Frequency tuning of the oscillatory network**



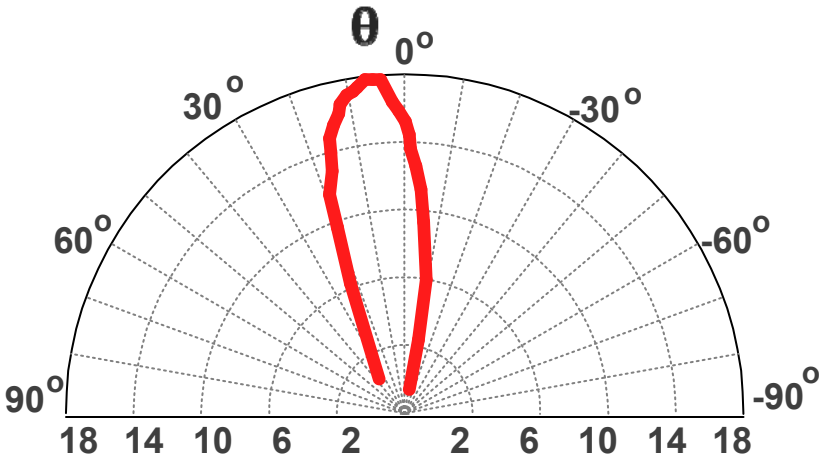
Beam Steering Measurement



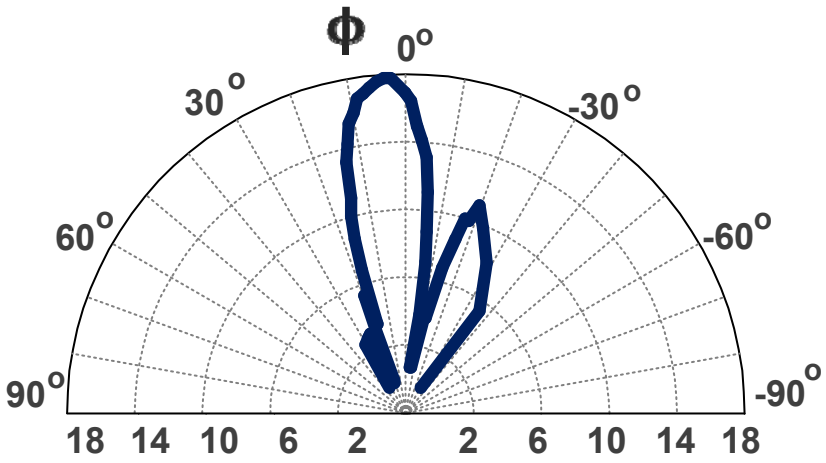


- RF to DC detector for pattern measurement:
  - Beam pattern
  - Antenna gain
  - 2D beam steering

Radiated Beam at 338GHz



Directivity in *theta* (dB)

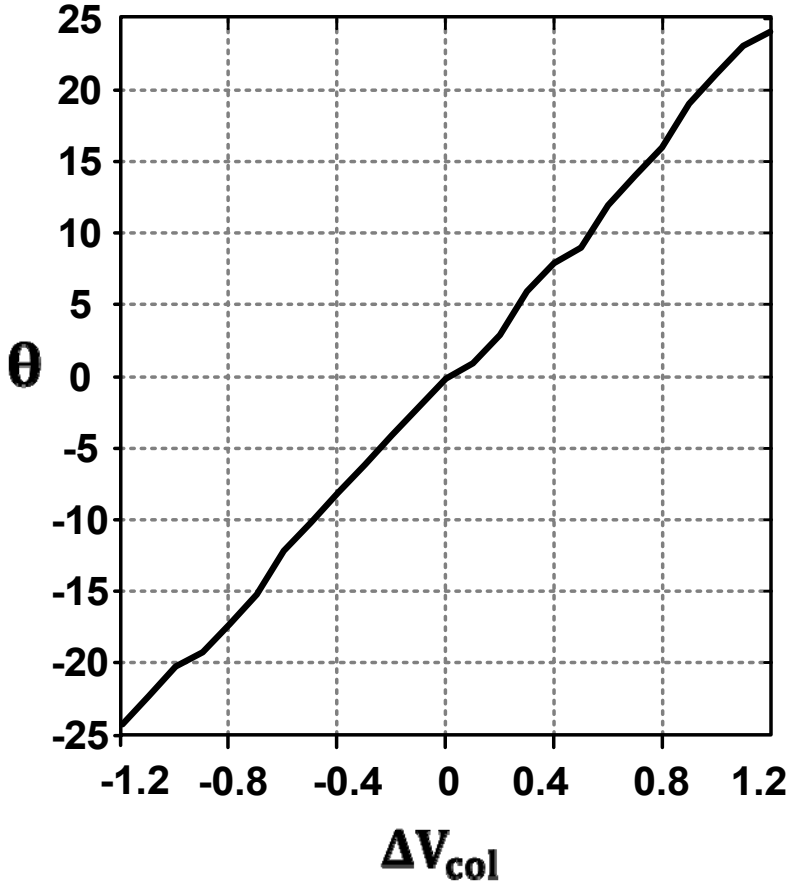


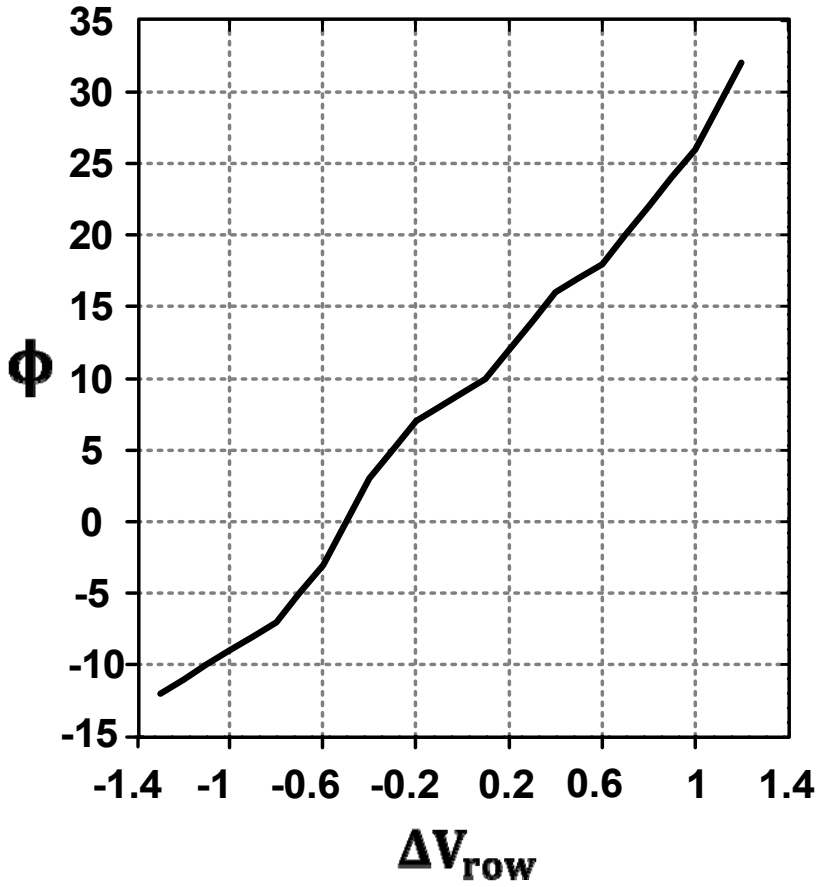
Directivity in *phi* (dB)

- **Measured -3dB beam width:**
  - $\Delta\varphi_{-3dB} = 24^{o}$
  - $\Delta\Theta_{-3dB} = 27^{o}$
- **Measured antenna directivity: 18dB**

Beam Steering

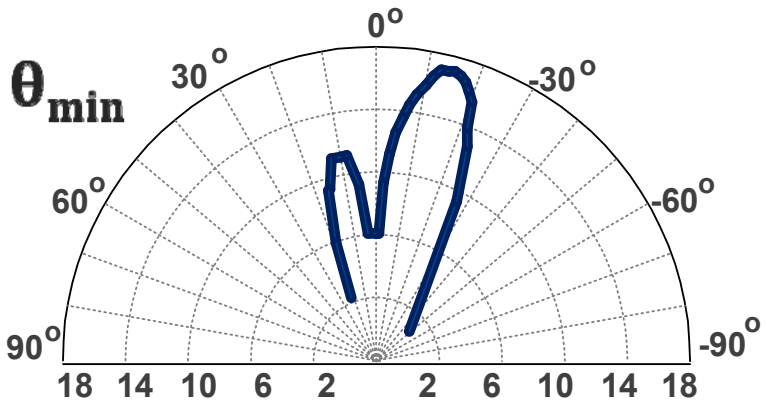
- Tuning coupler phase shift for beam steering

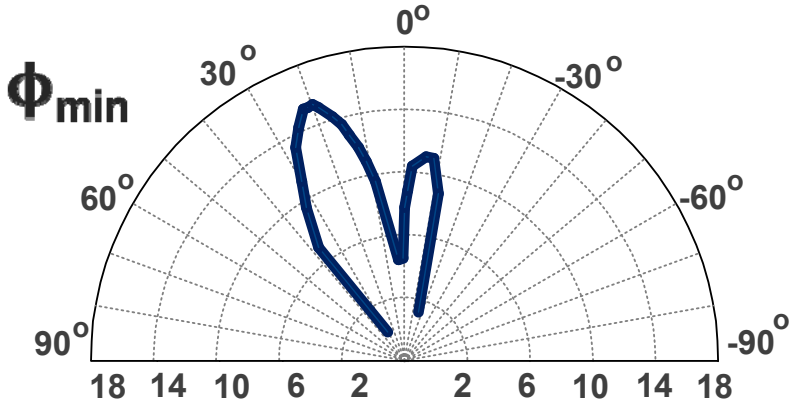


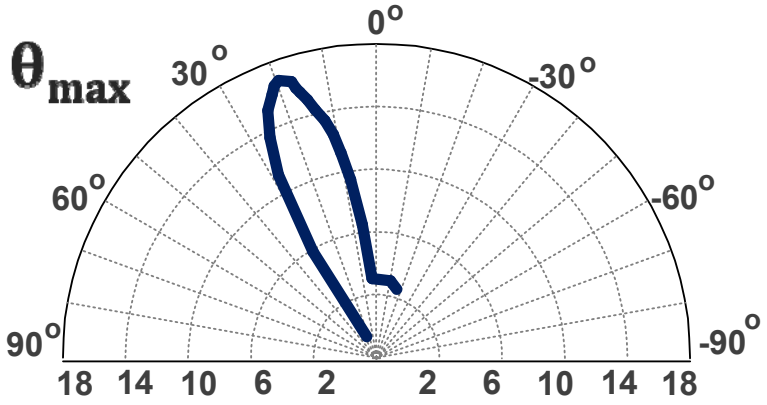


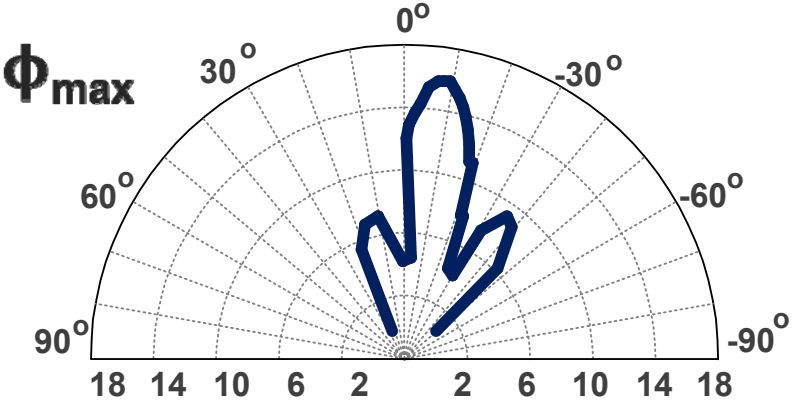
Measured Beam Steering

- **Beam scanning in orthogonal angles**

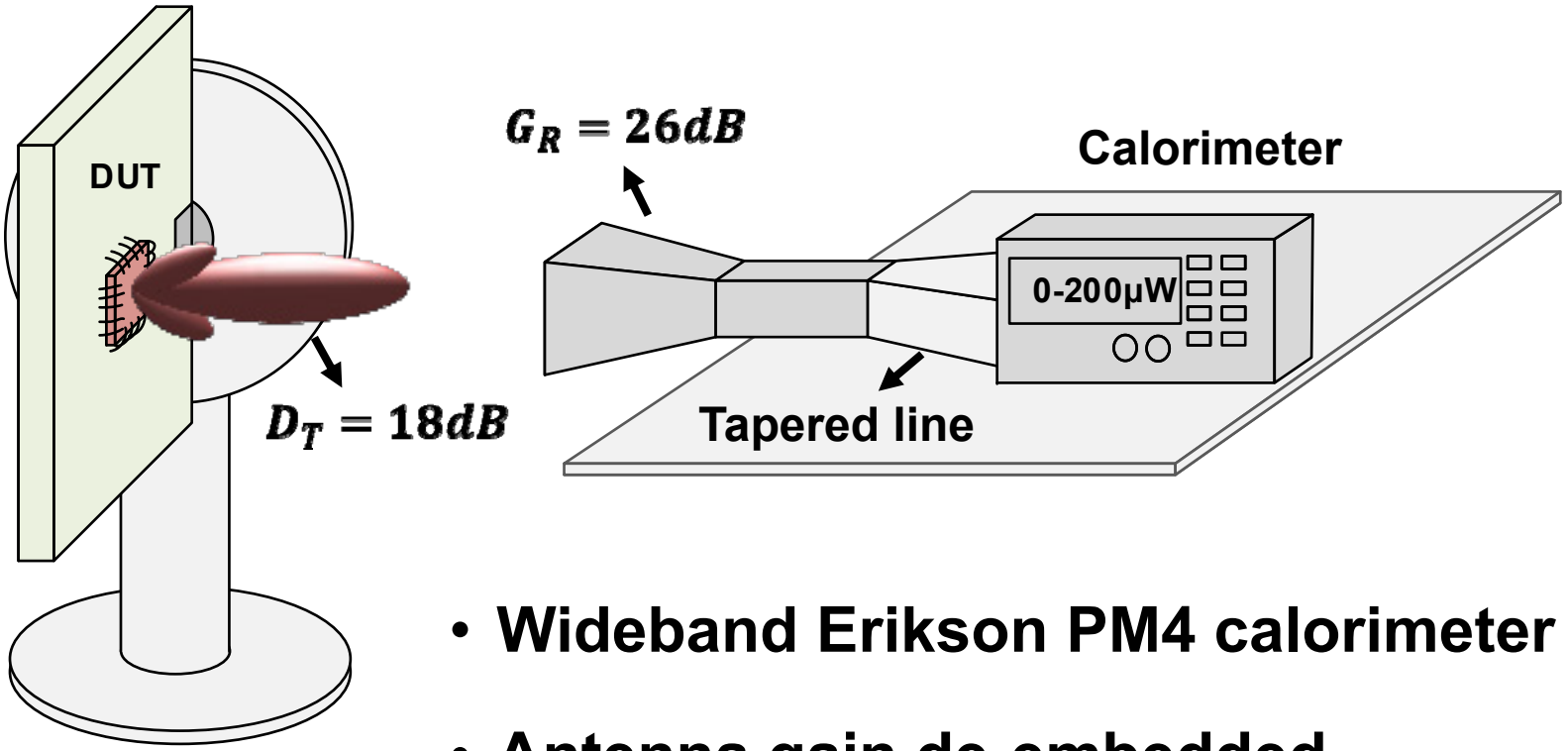








Radiated Power Measurement

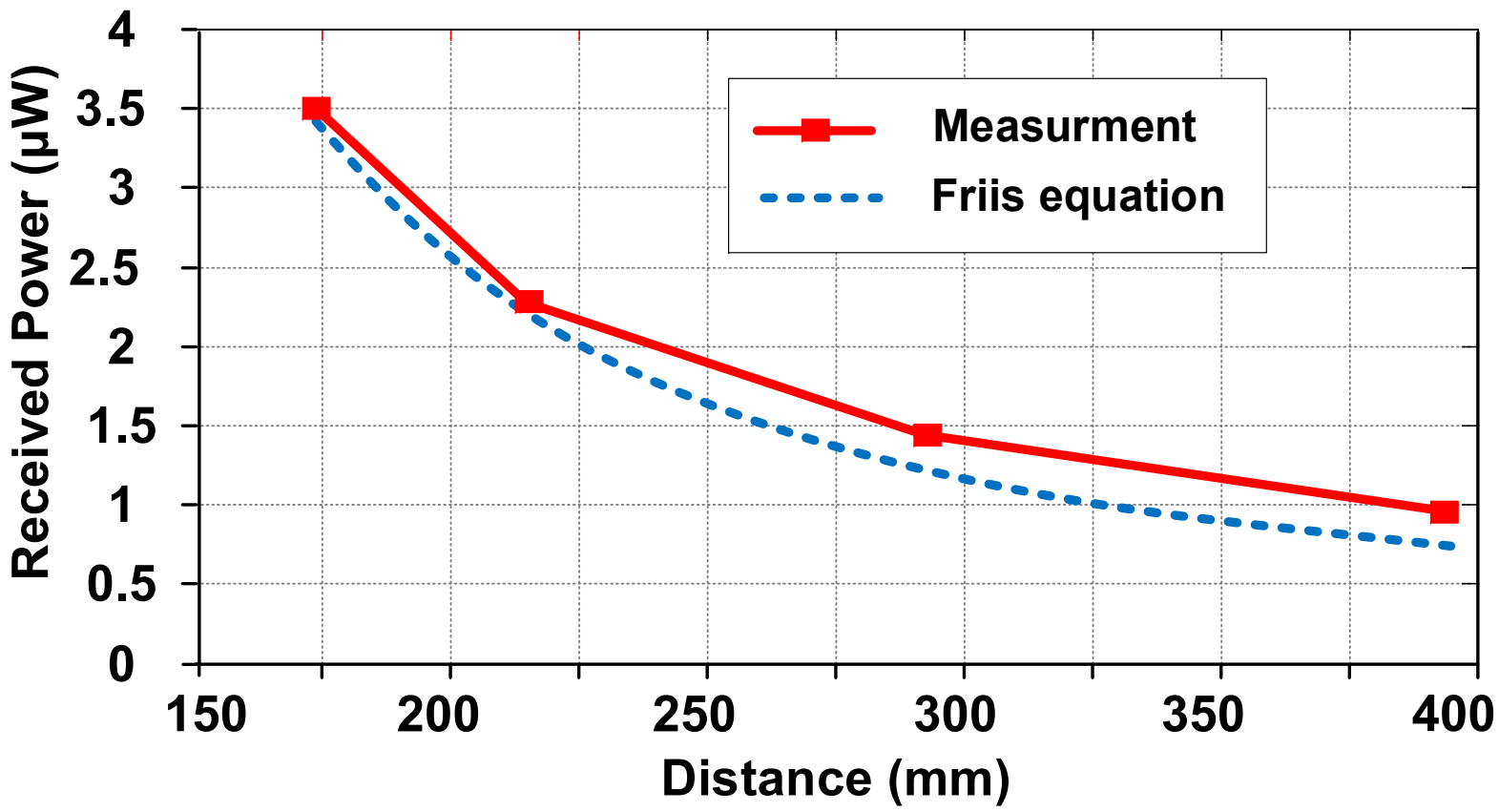


- Wideband Erikson PM4 calorimeter
- Antenna gain de-embedded

$$P_R = P_T - L + G_R + D_T$$

Power vs. Distance

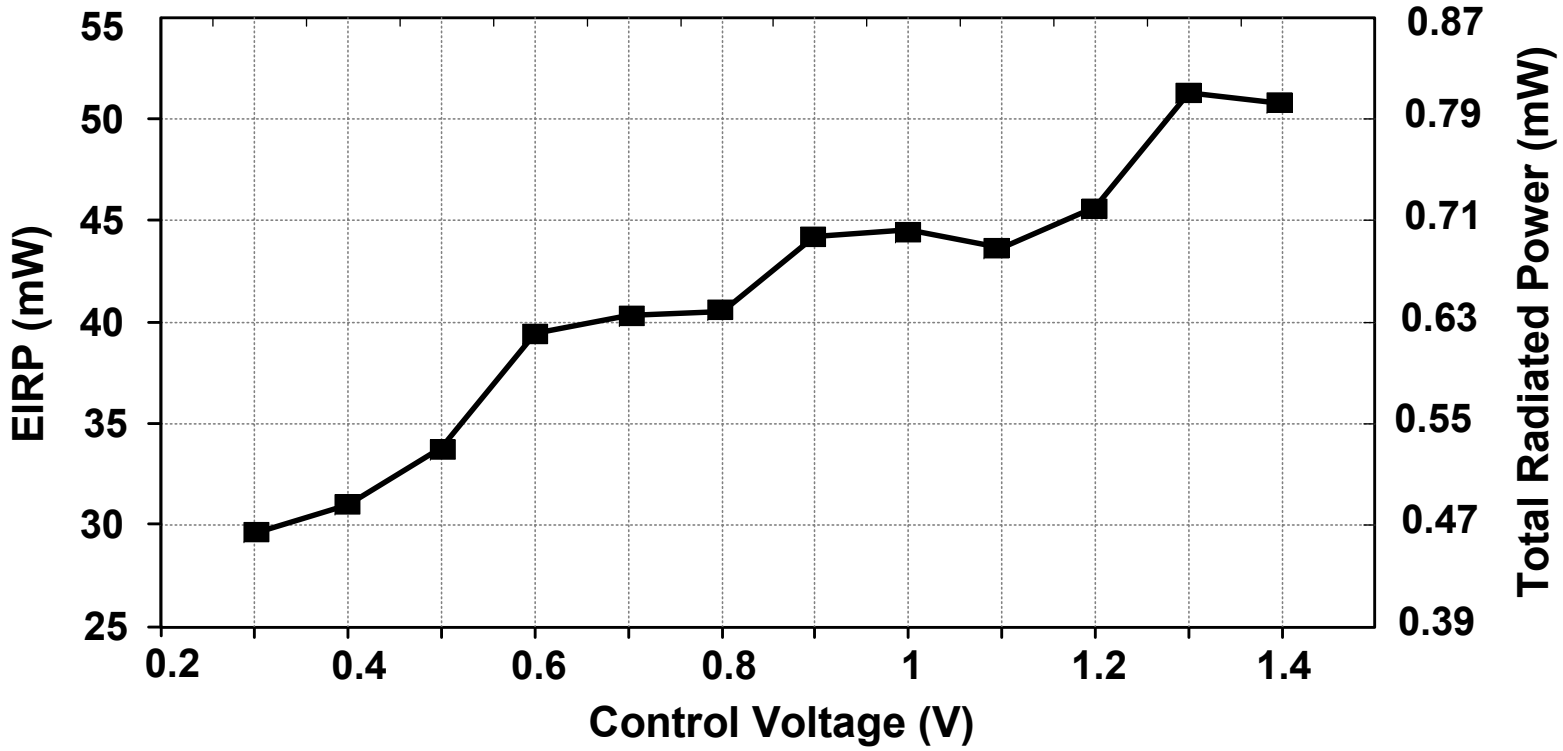
- Measured power and Friis equation verification



Radiated Power vs. Control

- **Total radiated power and EIRP:**

$$EIRP = P_R + L - G_R \qquad P_T = P_R + L - G_R - D_T$$



Performance Summary

Ref.	[1]	[2]	[3]	[4]	This Work
Frequency (GHz)	290	260	280	288	338
Total Power (dBm)	-1.2	0.5**	-7.2***	-4.1**	-0.9
Peak EIRP (dBm)	N/A*	15.7	9.4	N/A	17.1
Freq. Tuning (%)	4.5	1.4	3.2	Non-tuning	2.1
Phase Noise (@ 1MHz offset)	-78	-78.3	N/A	-87	-93
Beam Steering	N/A	Fixed pattern	80/80	Fixed pattern	45/50
DC Power (W)	0.33	0.8	0.81	0.28	1.54
Technology	65nm bulk CMOS	65nm bulk CMOS	45nm SOI CMOS	65nm bulk CMOS	65nm bulk CMOS
Area (mm^2)	0.36	2.25	7.2	0.32	3.9

* Power measured by probing
** A Hemispheric lens is used for back-side radiation
*** Substrate-thinning used for front-side radiation

Outline

- Introduction
- Theory of coupled oscillatory networks
- A 2D scalable terahertz phased array
- Circuit design and implementation
- Prototype measurement
- Conclusion

Conclusion

- Systematic method for THz generation and radiation
- High-power phased array for THz transceivers
- Scalable structure based on local coupling

Chip highlights:

- Highest frequency phased array
- Highest EIRP on CMOS above 100GHz
- Lowest phase noise on CMOS above 100GHz
- First THz phased array w/o post processing

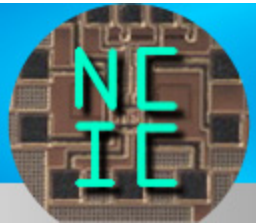
Acknowledgment

- NSF, ARL, and ONR for support
- Dr. Pauli Maki, Dr. Alfred Hung, and Dr. Joe Qiu
- TSMC University Shuttle Program
- Situne Corporation
- Virginia Diodes Inc.
- Prof. Steven Strogatz at Cornell
- Dr. M. Adnan, Dr. R. Han, H. Aghasi, and other members of UNIC lab

A 300GHz Frequency Synthesizer with 7.9% Locking Range in 90nm SiGe BiCMOS

Pei-Yuan Chiang[1] , Zheng Wang[1], Omeed Momeni[2], Payam Heydari[1]

[1]University of California, Irvine, CA
[2]University of California, Davis, CA



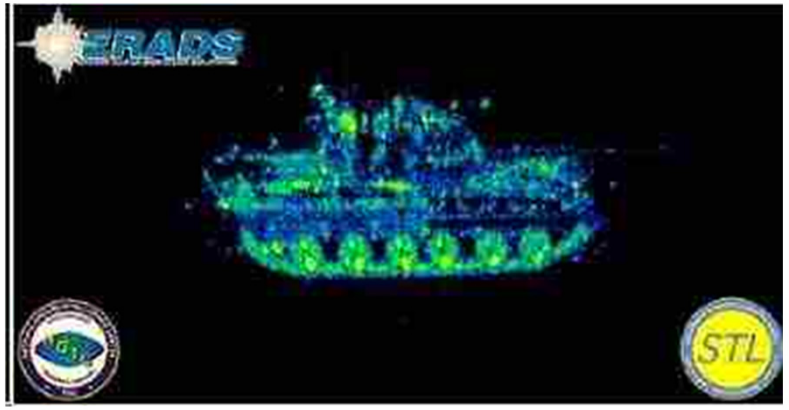
Outline

- Motivation
- World's First 300 GHz Synthesizer in Silicon
  - Triple-Push VCO
  - Three-Phase Injection-Locked Divider (÷4)
- Experimental Results
- Conclusions

Terahertz Applications

- Molecular spectroscopy (molecular modeling/identification, bio-detection)
- Short-range 10+ gigabit wireless communications
- Radar imaging (concealed weapon detection, illicit drugs)

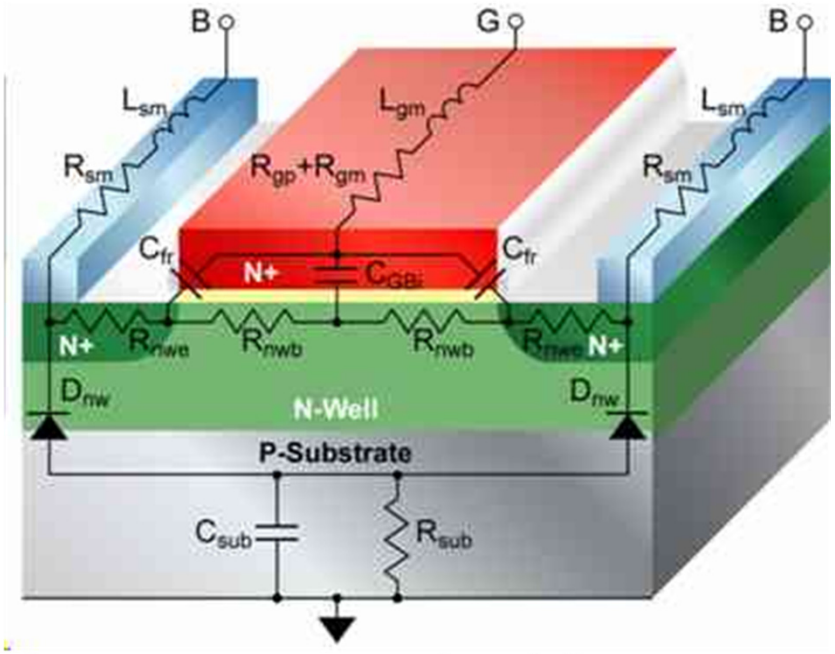
Synthesizer is an essential block in these applications



Thomas M. Goyette *et al*., "THz Compact Range Radar Systems," *IEEE Int. Microwave Symp.*, June, 2003

Challenges

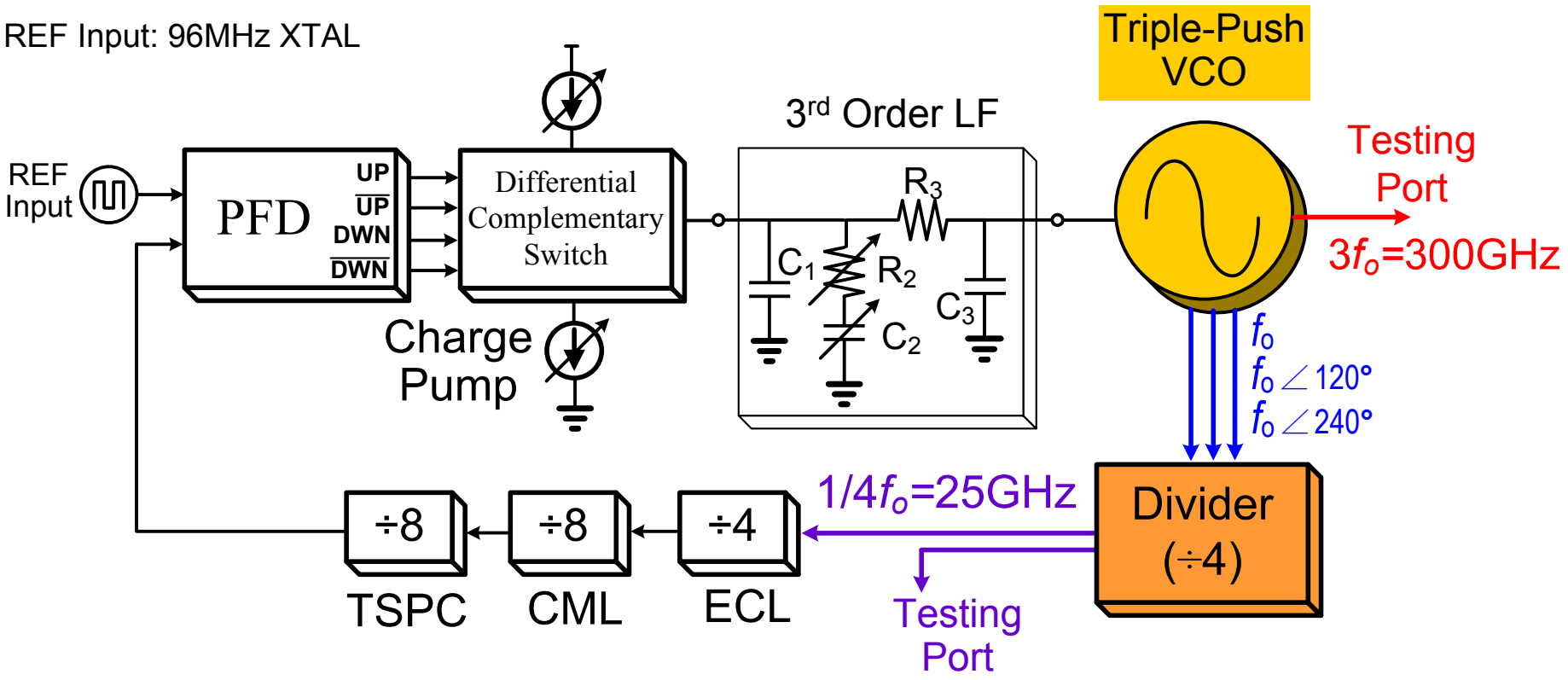
- The operation frequency too close to the maximum oscillation frequency (f_{MAX}) of transistors
- Severe loss (low *Q* factor) and small C_{MAX}/C_{MIN} ratio of varactors at THz frequencies
- Limited divider operation frequency and input sensitivity



Cross section of MOS Varactor

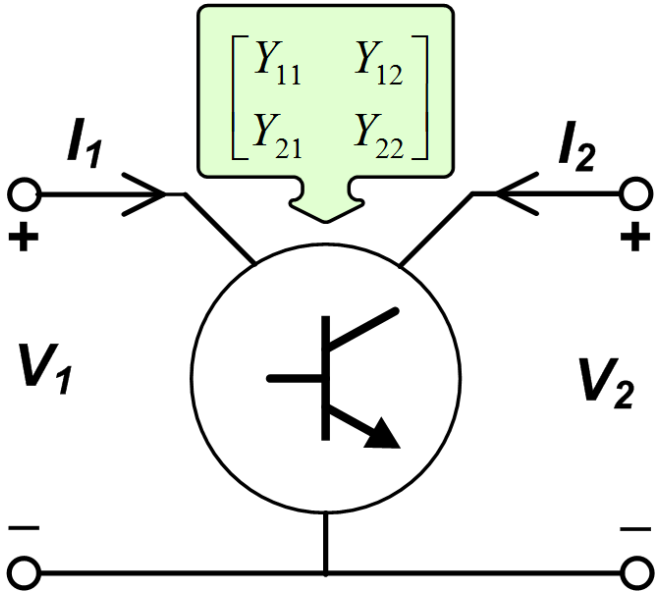
TowerJazz, Inc., "*Modeling Design Manual for the SBC18 Family_Rev_13*"

300GHz Synthesizer



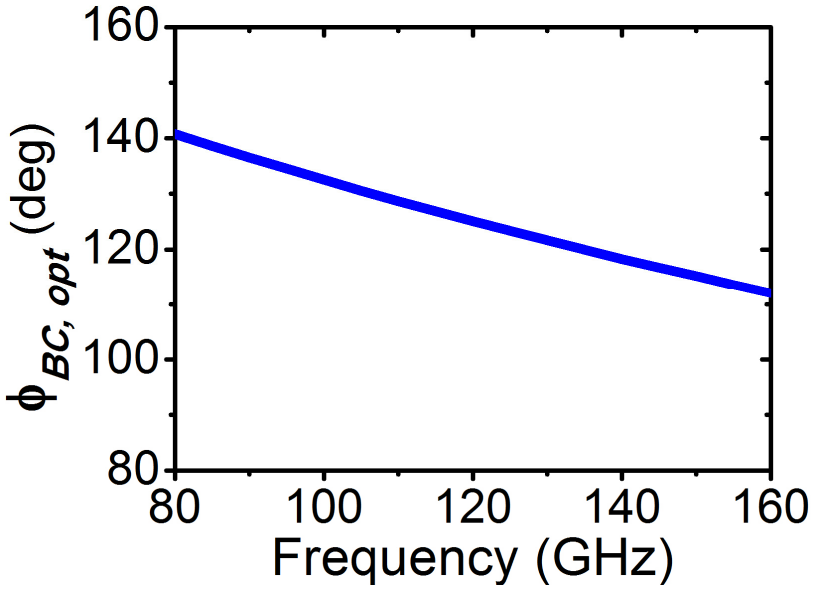
- **The synthesizer employs a 3rd-order LF, a triple-push VCO, and a divide-by-1024**
- **The loop is locked to the VCO's fundamental at 100 GHz**
- **With three-phase injection, the divider achieves wider locking range**

Transistor Optimum Condition



$$A = \left|\frac{V_2}{V_1}\right|$$

$$\phi_{BC} = \angle\left(\frac{V_2}{V_1}\right)$$



$$P_N = |V_1|^2 \left[\underbrace{(G_{11} + A^2 G_{22})}_{P_R} + \underbrace{A\left|Y_{12} + Y_{21}^*\right| \cos\left(\angle(Y_{12} + Y_{21}^*) + \phi_{BC}\right)}_{P_G} \right]$$

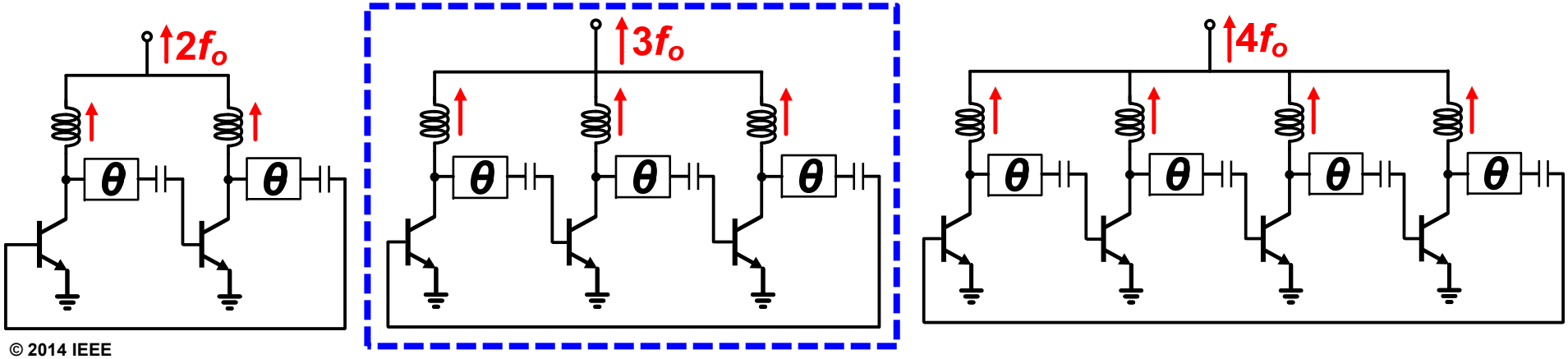
Maximum $|P_G|$ ⇒ $\phi_{BC,opt} = (2k+1)\pi - \angle(Y_{12} + Y_{21}^*)$

O. Momeni and E. Afshari, "High power terahertz and millimeter-wave oscillator design: A systematic approach," *JSSC*, vol. 46, pp. 583–597, March 2011

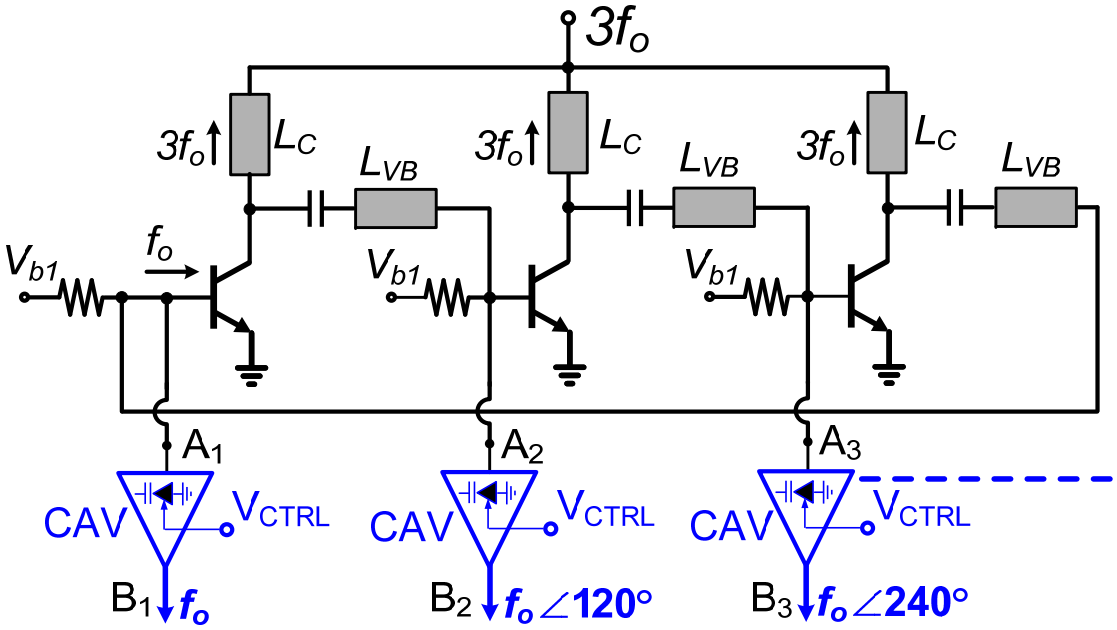
Design Considerations in Ring Osc.

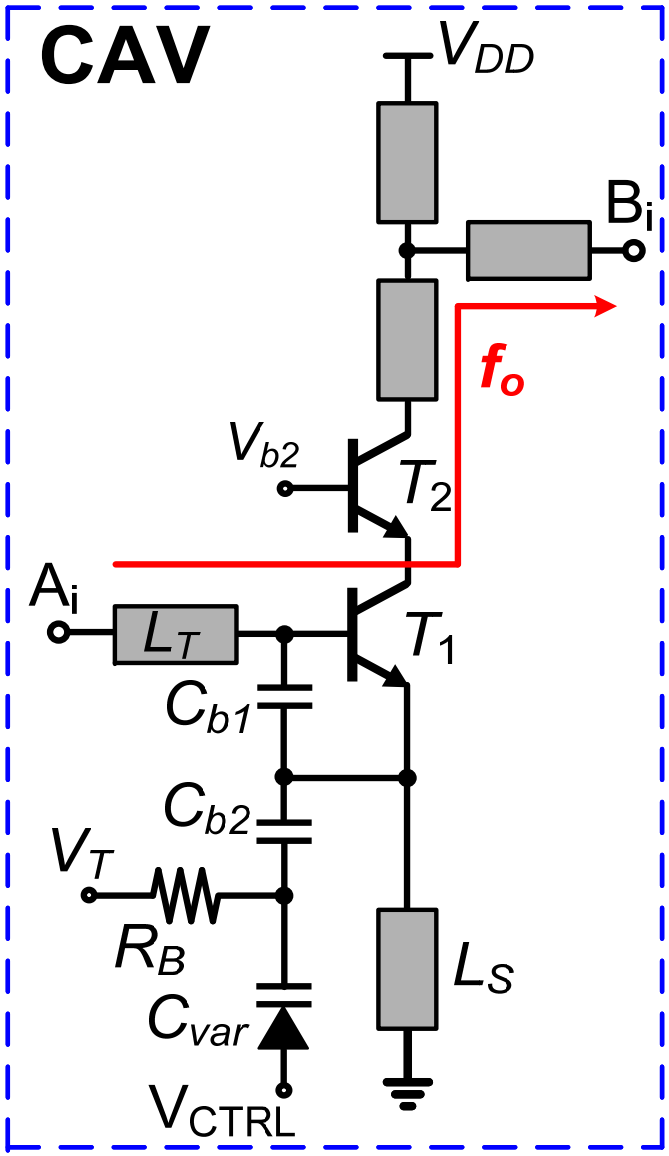
Assume output frequency of 300 GHz

	2-stage osc.	3-stage osc.	4-stage osc.
f_{osc}(GHz) / ϕ_{opt}	150 / 115°	100 / 130°	75 / 143°
Additional θ between each stage	65°	10°	53°
Number of transistors	2	3	4



Triple-Push VCO with CAV (1)



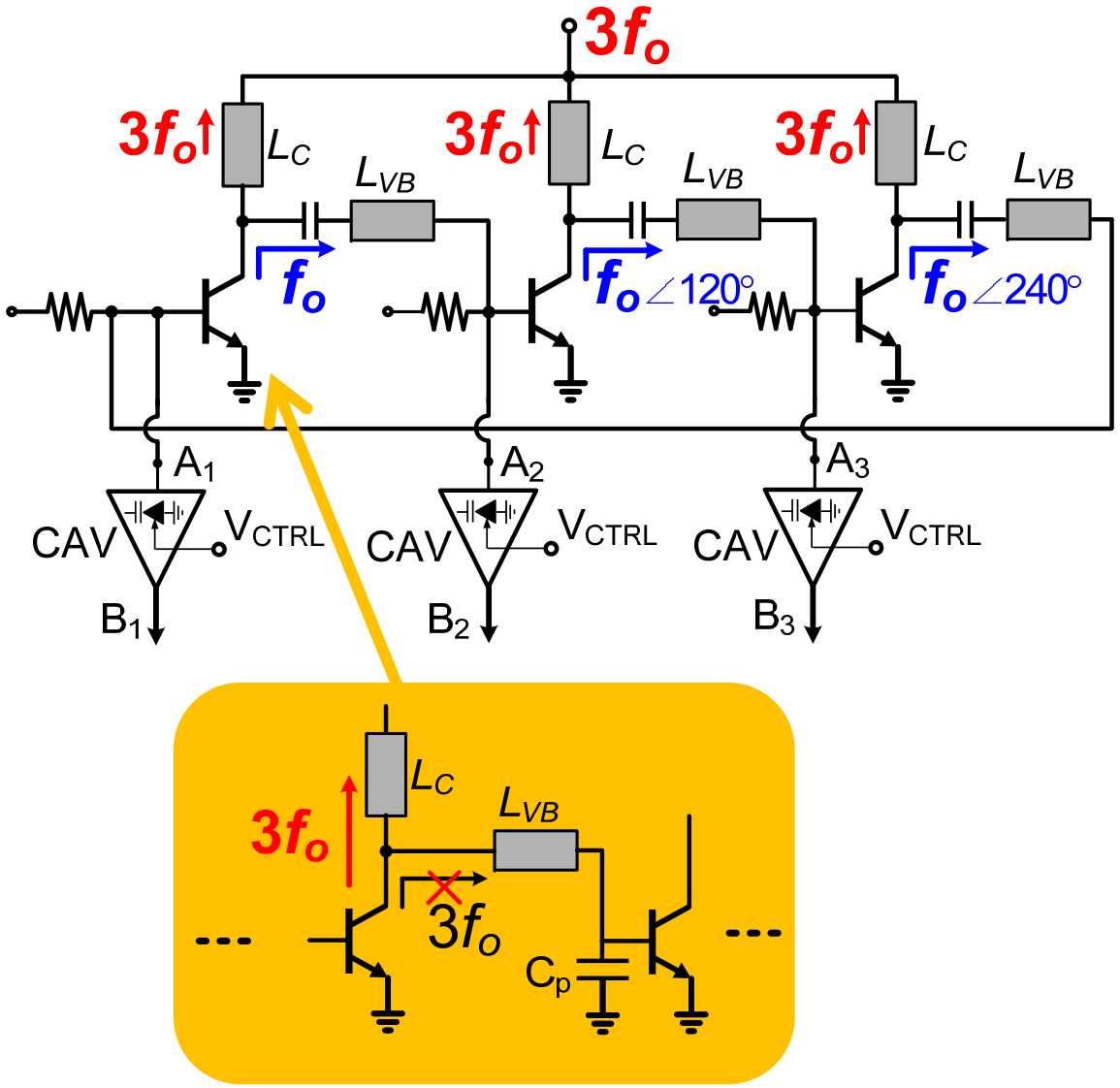


CAV: Colpitts-based Active Varactor

CAV:

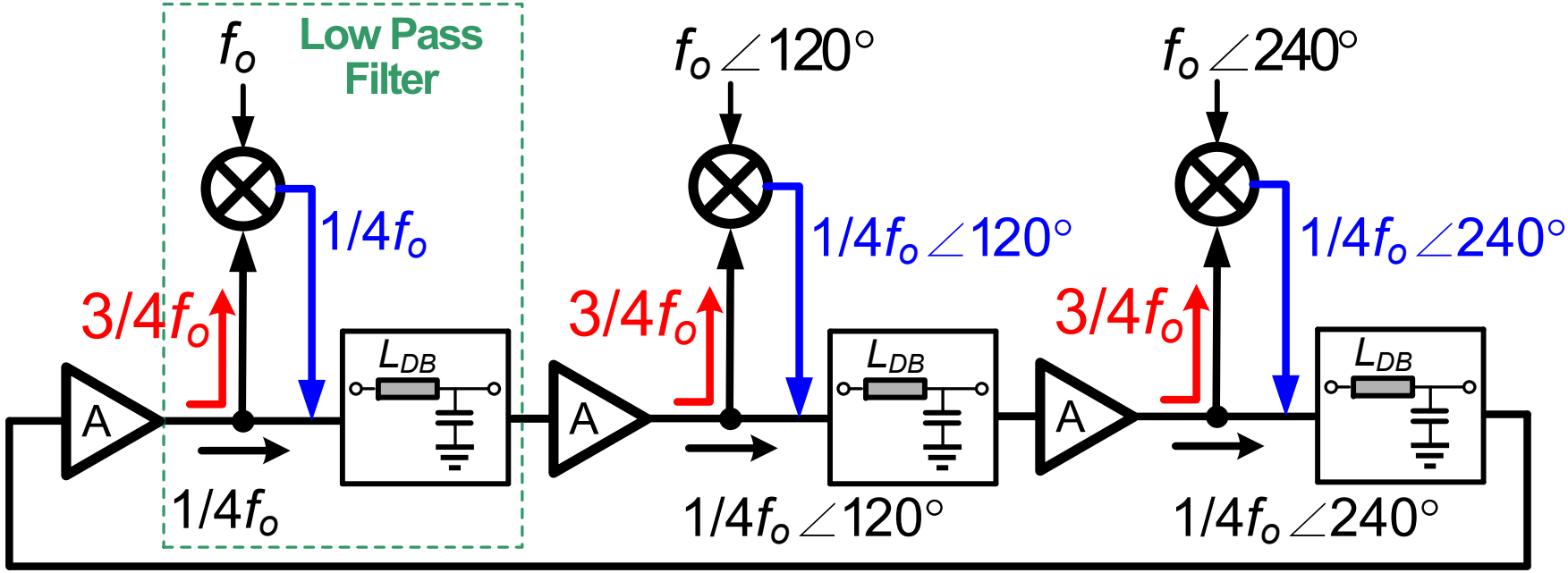
- Compensates for the varactor loss (C_{var})
- Provides tunable capacitance to the ring
- Buffers and injects f_o to the divider (÷4)

Triple-Push VCO with CAV (2)



- f_o experiences 120° phase-delay from the input to the output of each stage
- $3f_o$'s are added in-phase at the common node
- L_{VB} introduces extra phase-shift to achieve $\phi_{BC,opt}$
- L_{VB} enhances coherent power summation at $3f_o$

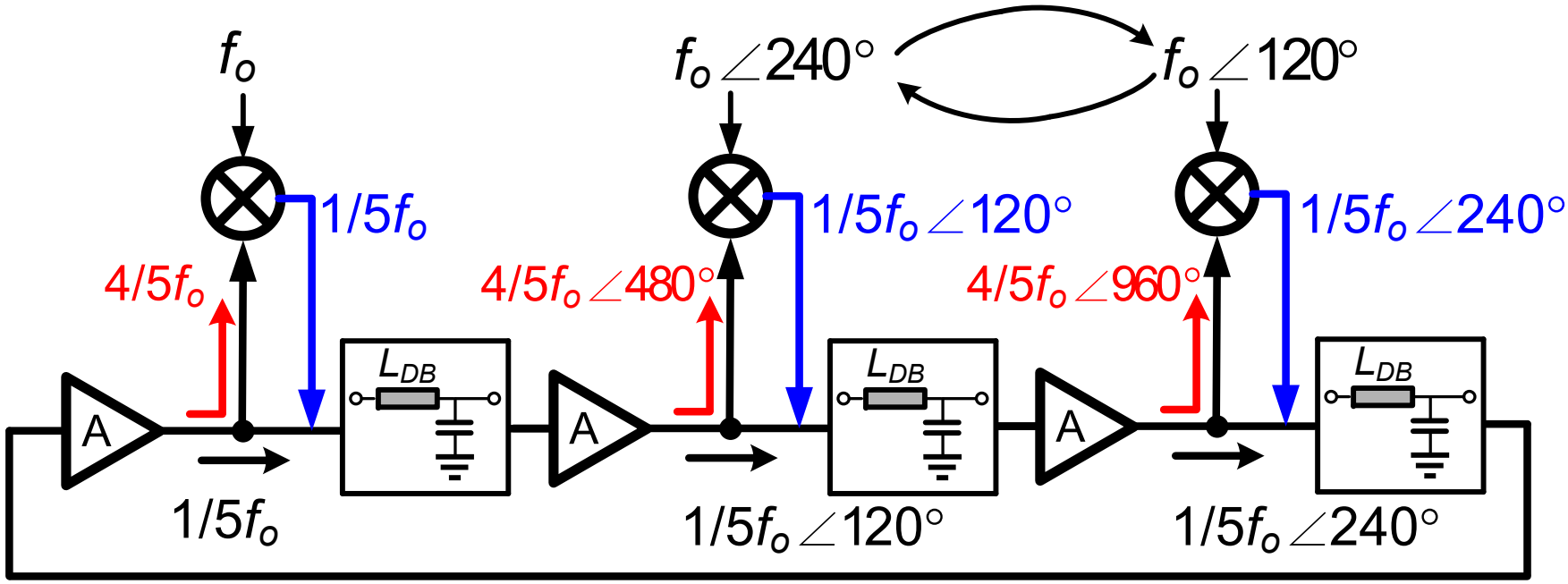
Conceptual Divider Loop (÷4)



- **The free-running frequency of the divider loop is close to $1/4f_o$**
- **$3/4f_o$ generated from the amplifier A is mixed with the three-phase input signal**
- **The loop is locked to $1/4f_o$, i.e., frequency difference component**

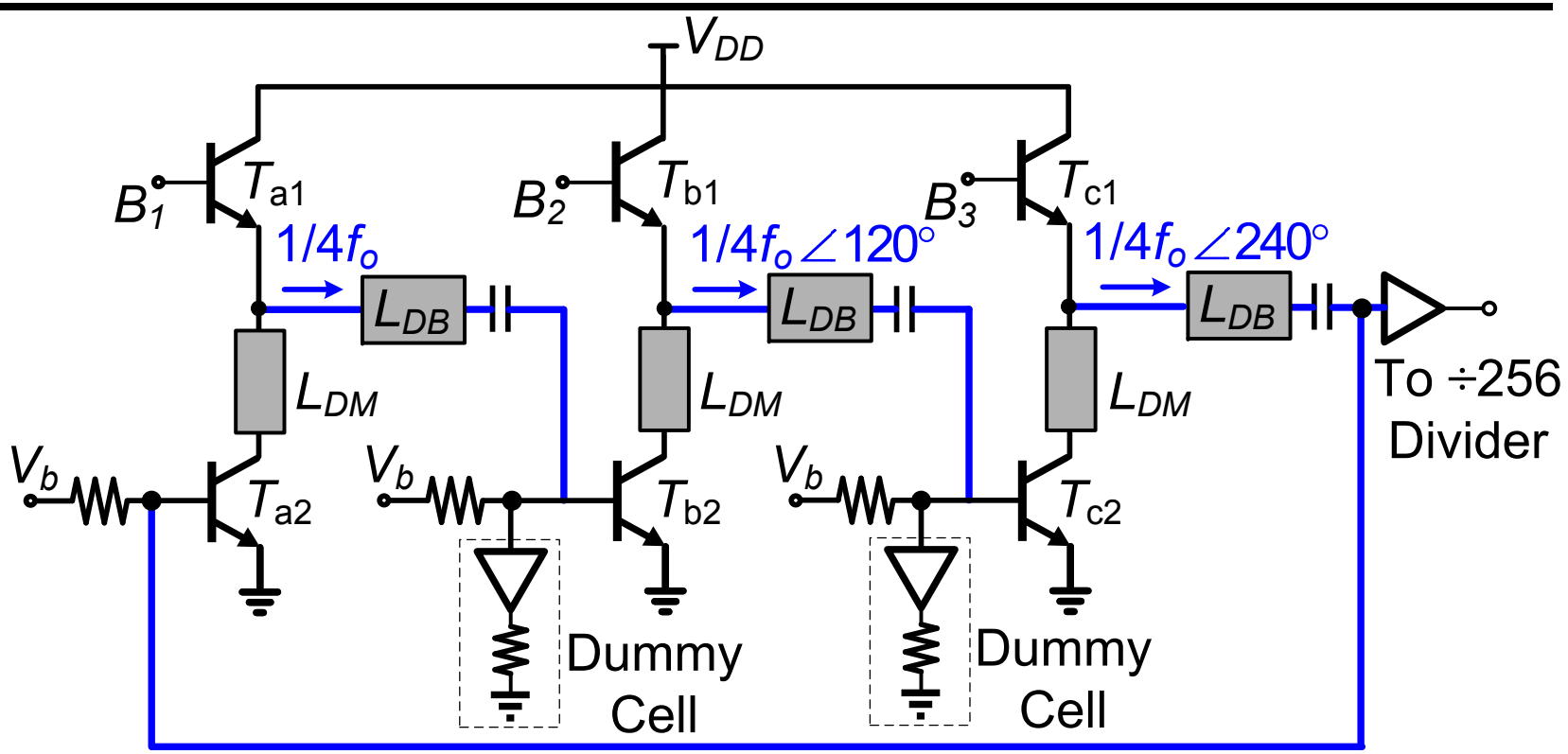
A. Mirzaei *et al*., "Injection-locked frequency dividers based on ring oscillators with optimum injection for wide lock range," in *Proc. IEEE Symp. VLSI Circuits*, Sep. 2006, pp. 174–175

Conceptual Divider Loop (÷5)



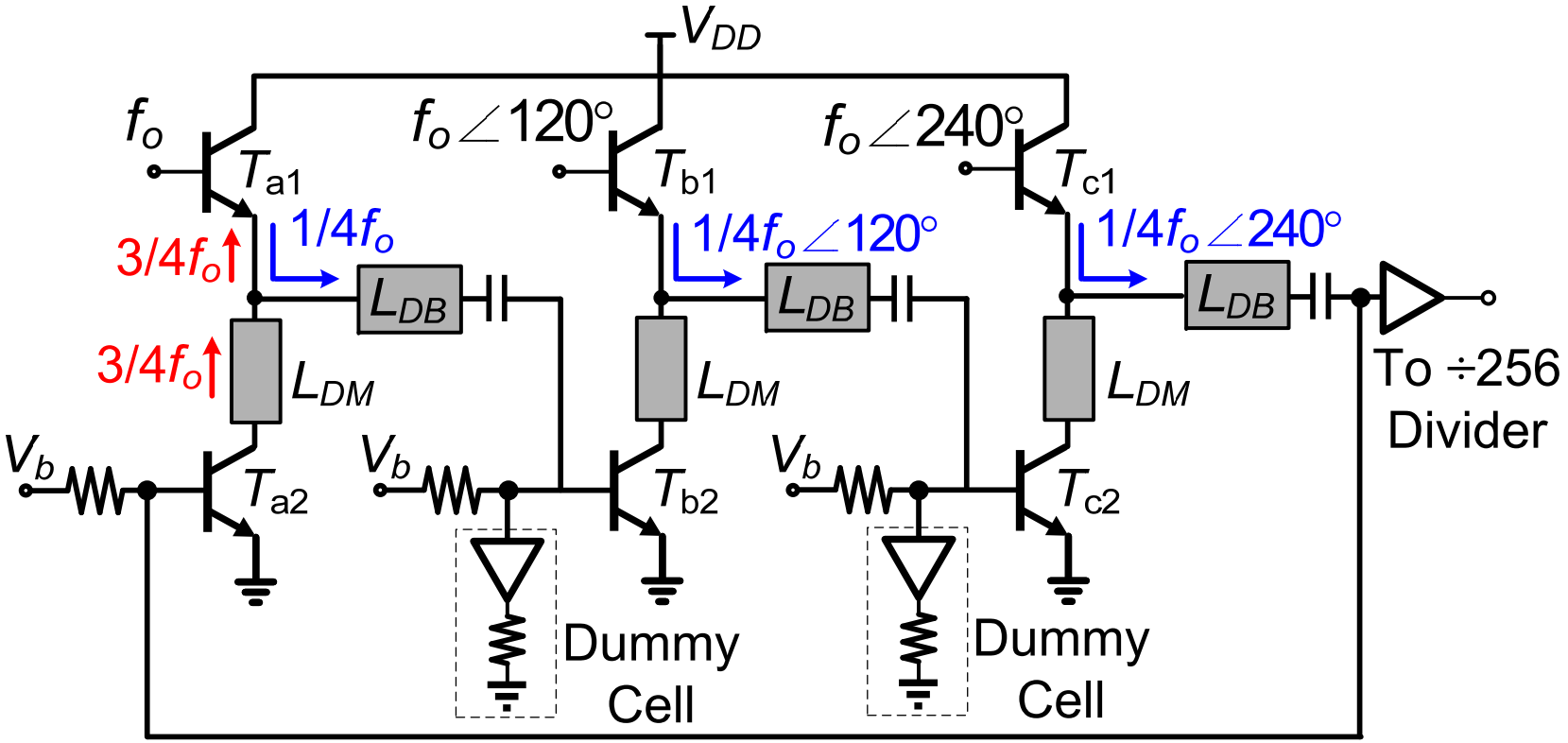
- Swap the last two input signals
- The three-phase input signals are mixed with the fourth harmonics
- The loop will be locked to $1/5f_o$ and perform divide-by-five

Injection-Locked Divider (÷4)



- The transistors T_{a1}~T_{c1} are acting as the mixing cells
- The $3/4f_o$ is mixed with input f_o and its output $1/4f_o$ flows back to the loop
- L_{DB} forces $3/4f_o$ to flow into the mixer and improves mixing efficiency

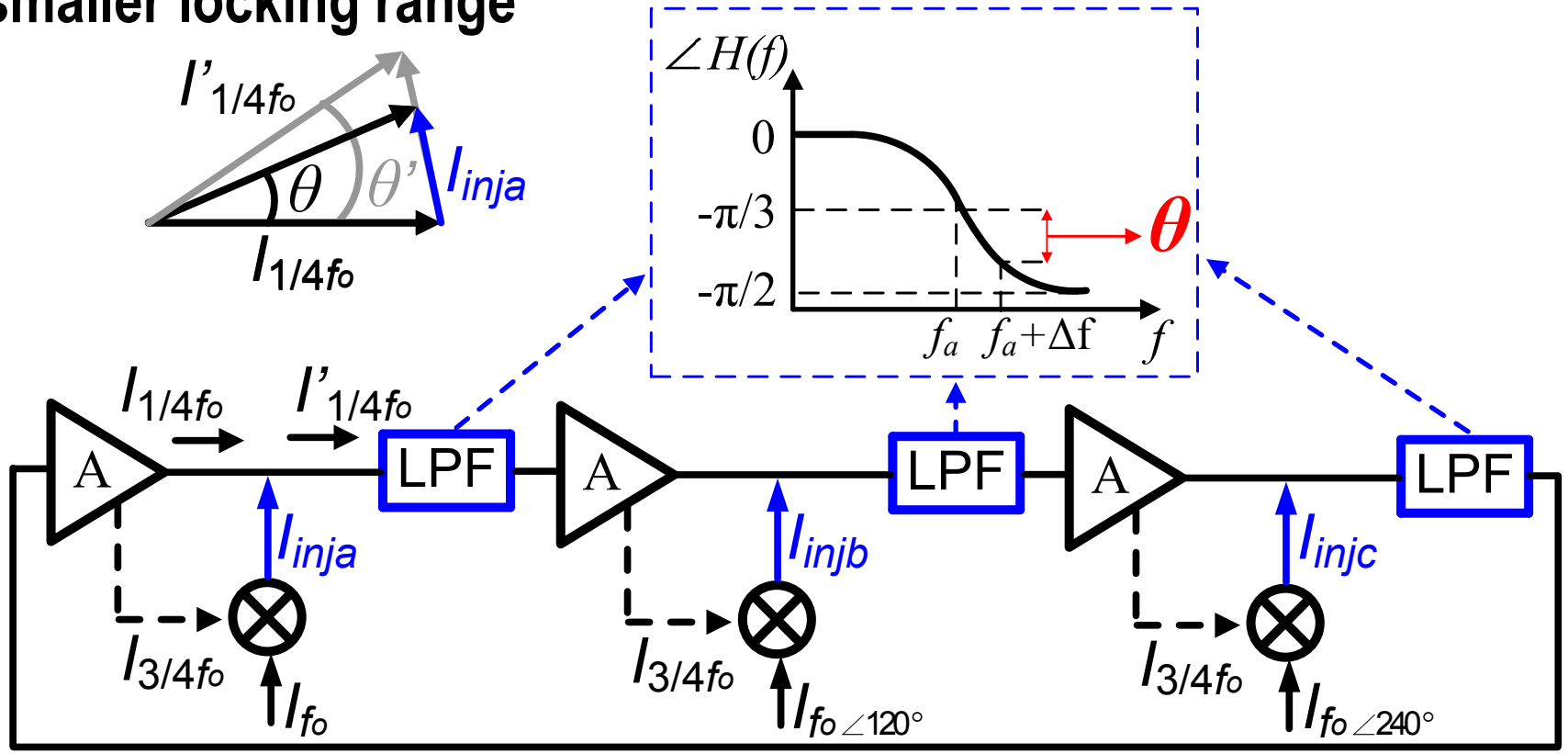
Injection-Locked Divider (÷4)



- The transistors T_{a1}~T_{c1} are acting as the mixing cells
- The $3/4f_o$ is mixed with input f_o and its output $1/4f_o$ flows back to the loop
- L_{DB} forces $3/4f_o$ to flow into the mixer and improves mixing efficiency

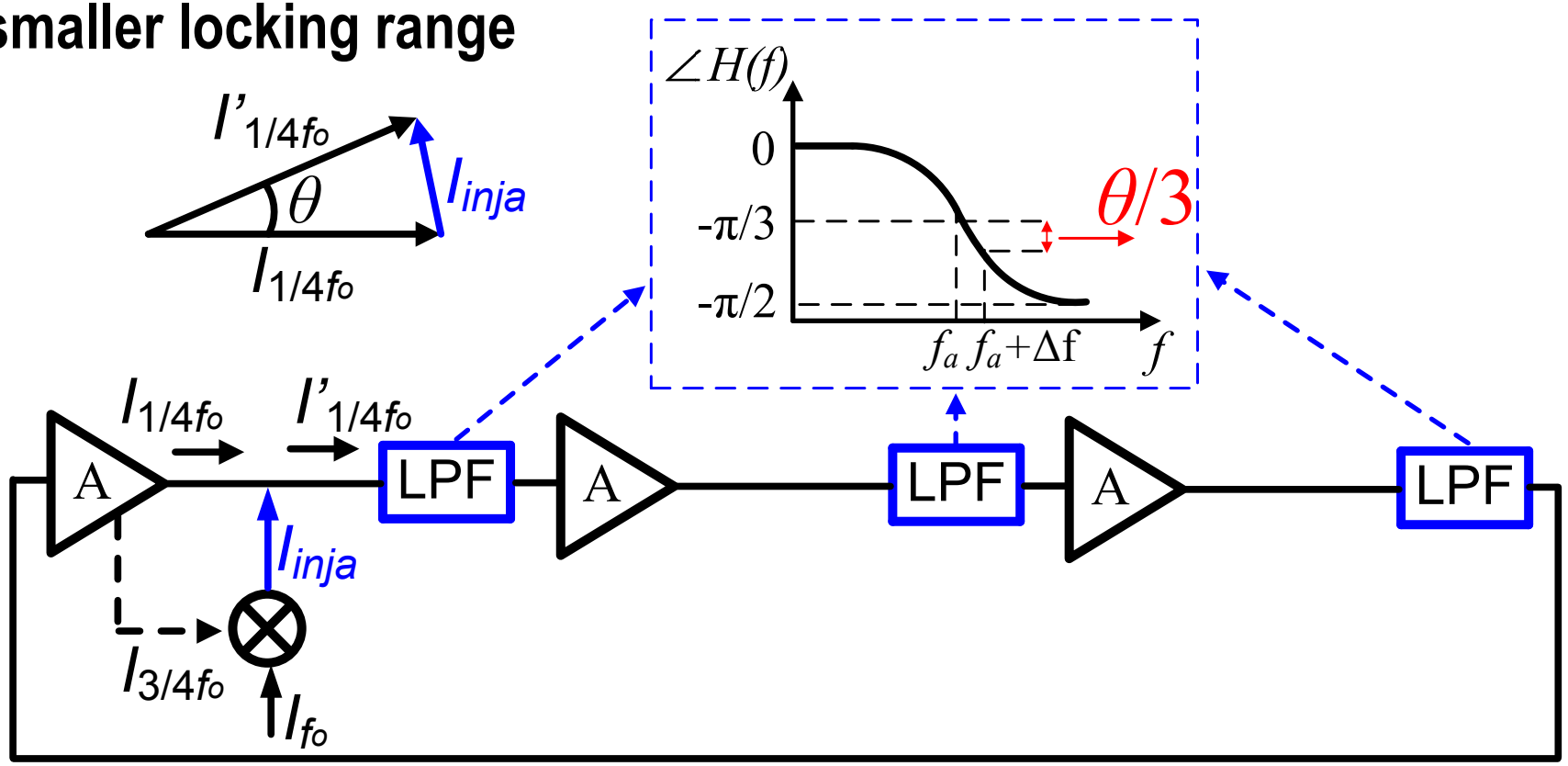
Three-Phase Injection

- For three-phase injection, the injection current of each stage introduces a phase change θ, and each LPF compensates for it, resulting in a frequency change
- For a single injection, each LPF only compensates for $\theta/3$, i.e., smaller locking range

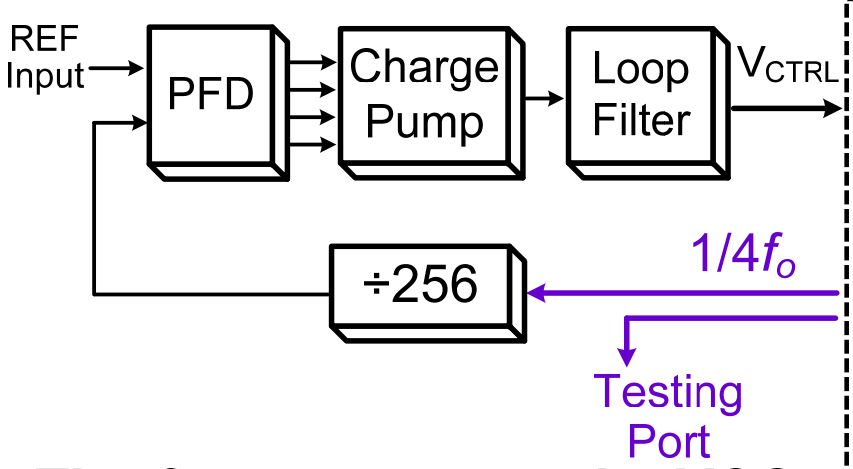


Three-Phase Injection

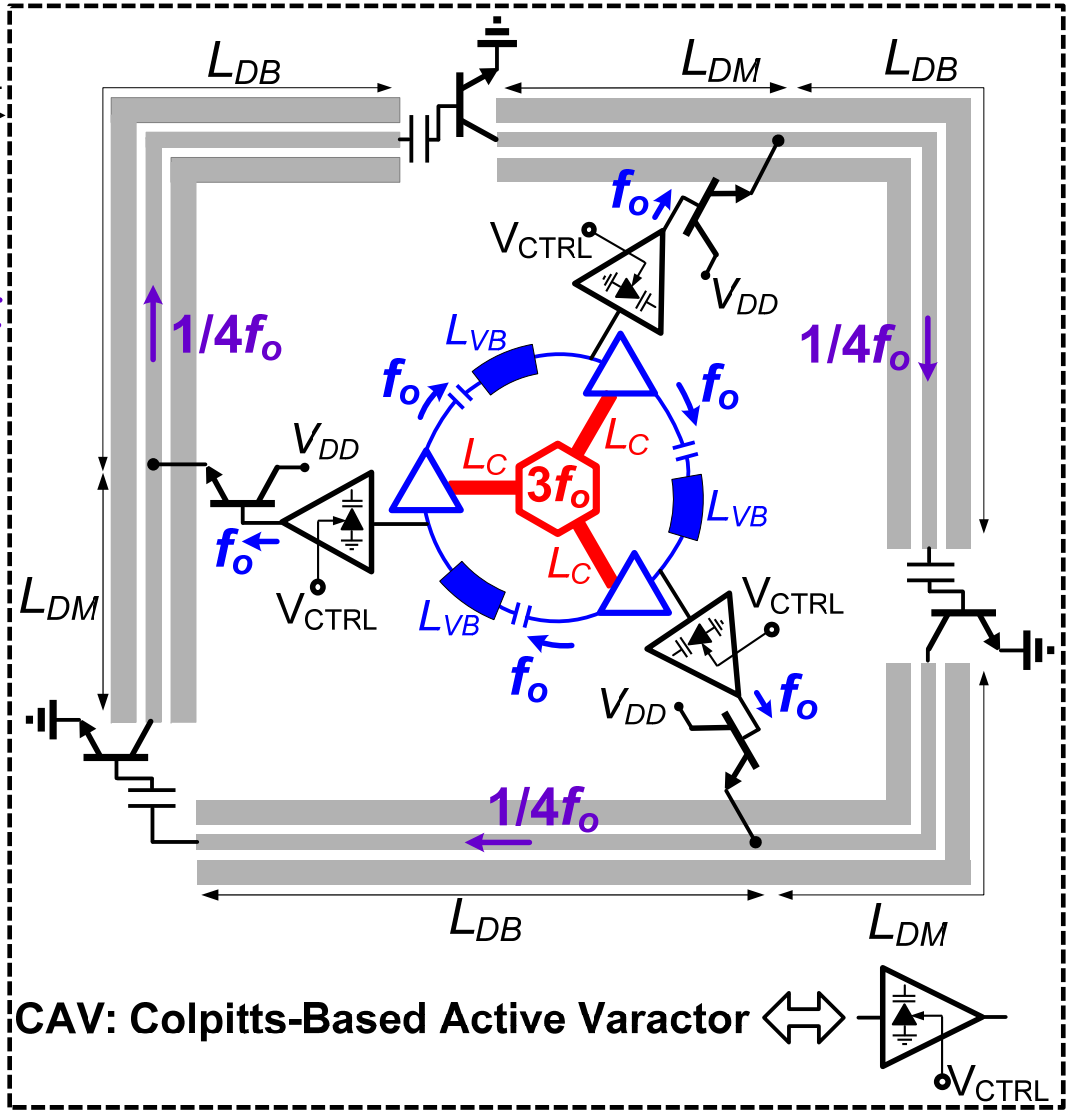
- For three-phase injection, the injection current of each stage introduces a phase change θ, and each LPF compensates for it, resulting in a frequency change
- For a single injection, each LPF only compensates for $\theta/3$, i.e., smaller locking range



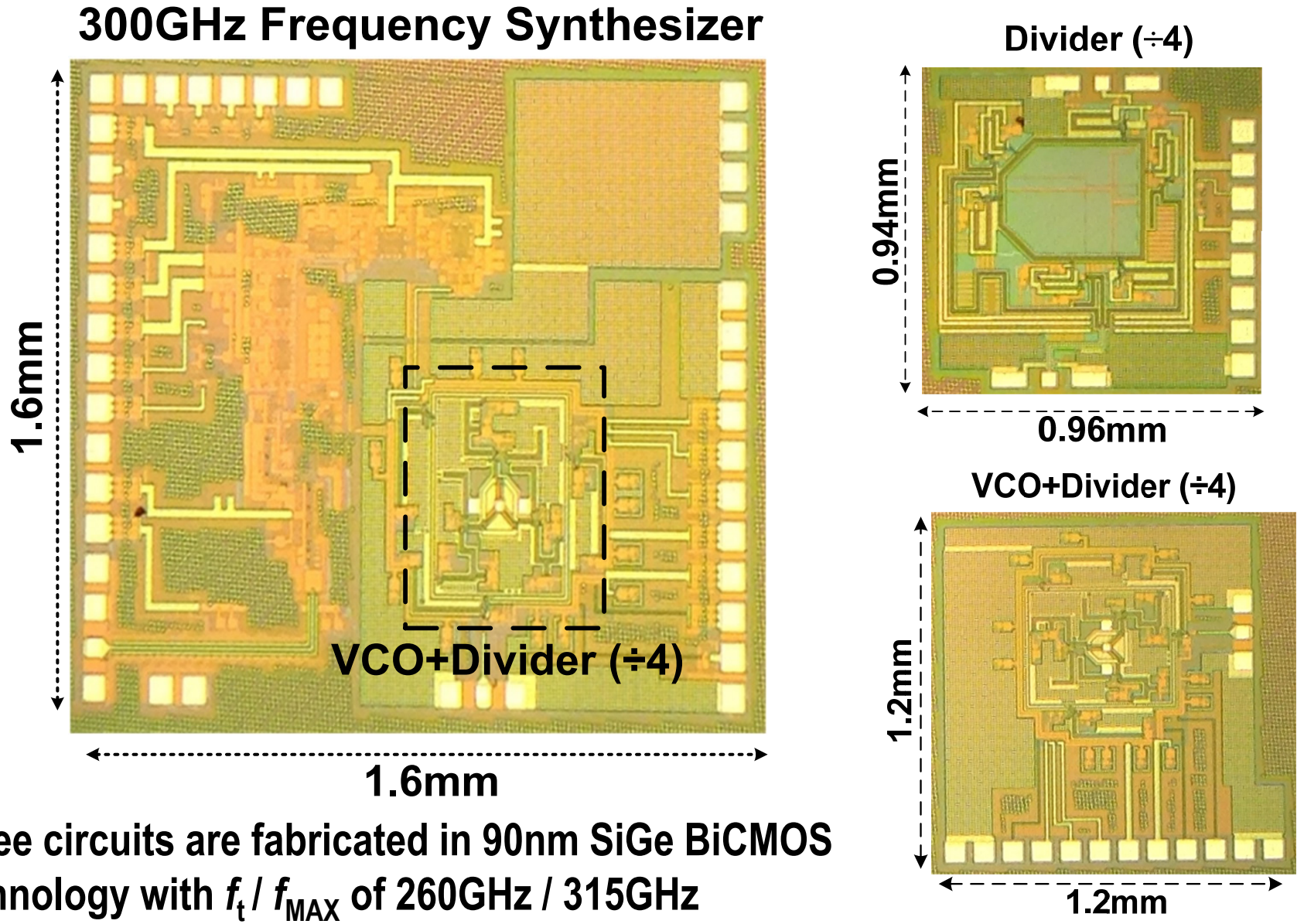
VCO/Divider Co-Design



- The f_o travels along the VCO ring and its 3rd harmonics are added at the center $3f_o$
- Widening its T-line, makes L_{VB} to fit to the VCO ring
- The synthesizer close loop behavior is verified by using $3f_o$ and $1/4f_o$ outputs

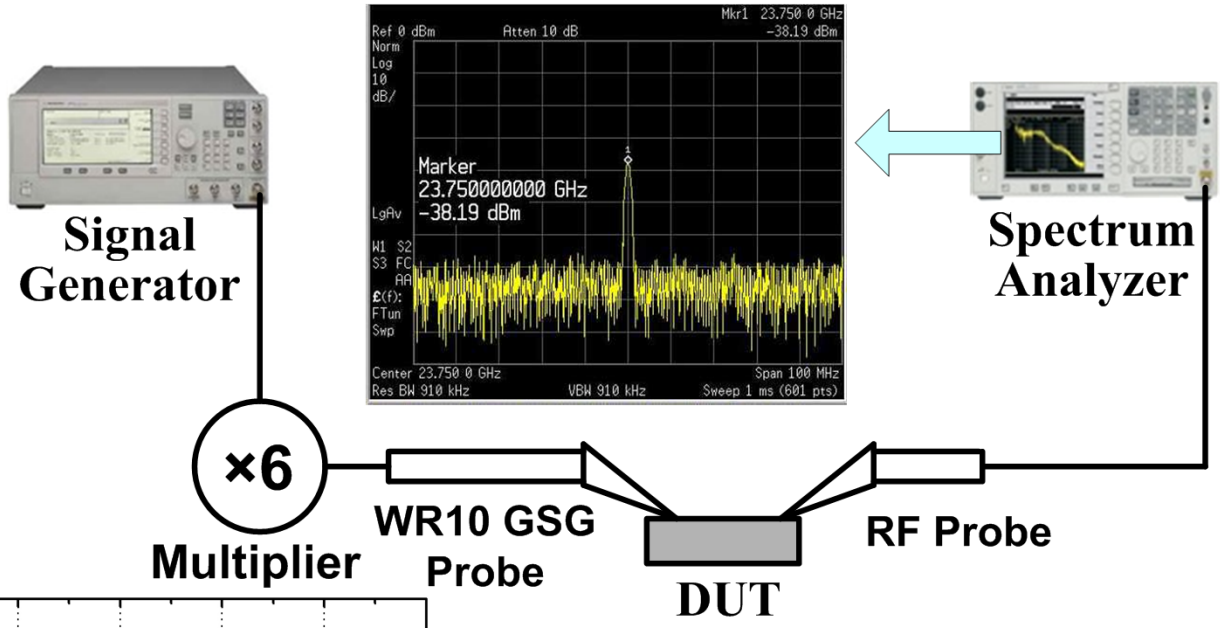


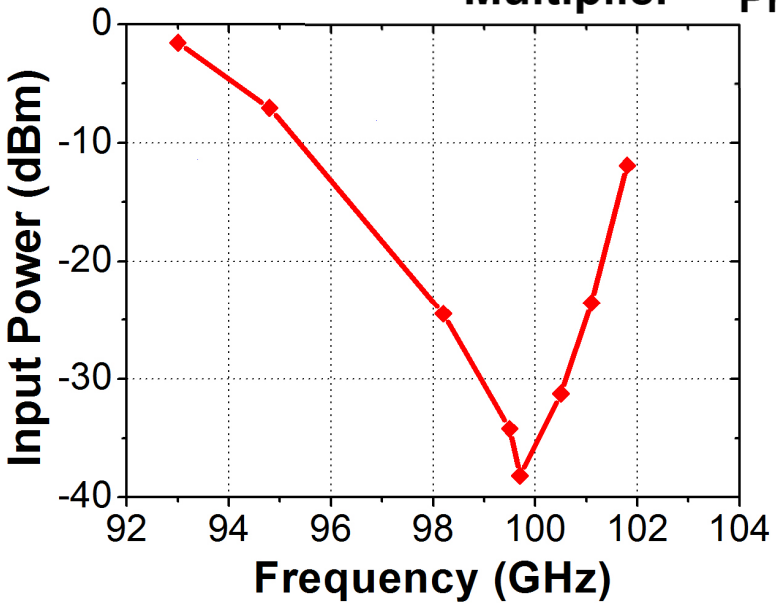
Chip Photograph



- Three circuits are fabricated in 90nm SiGe BiCMOS technology with f_t / f_{MAX} of 260GHz / 315GHz

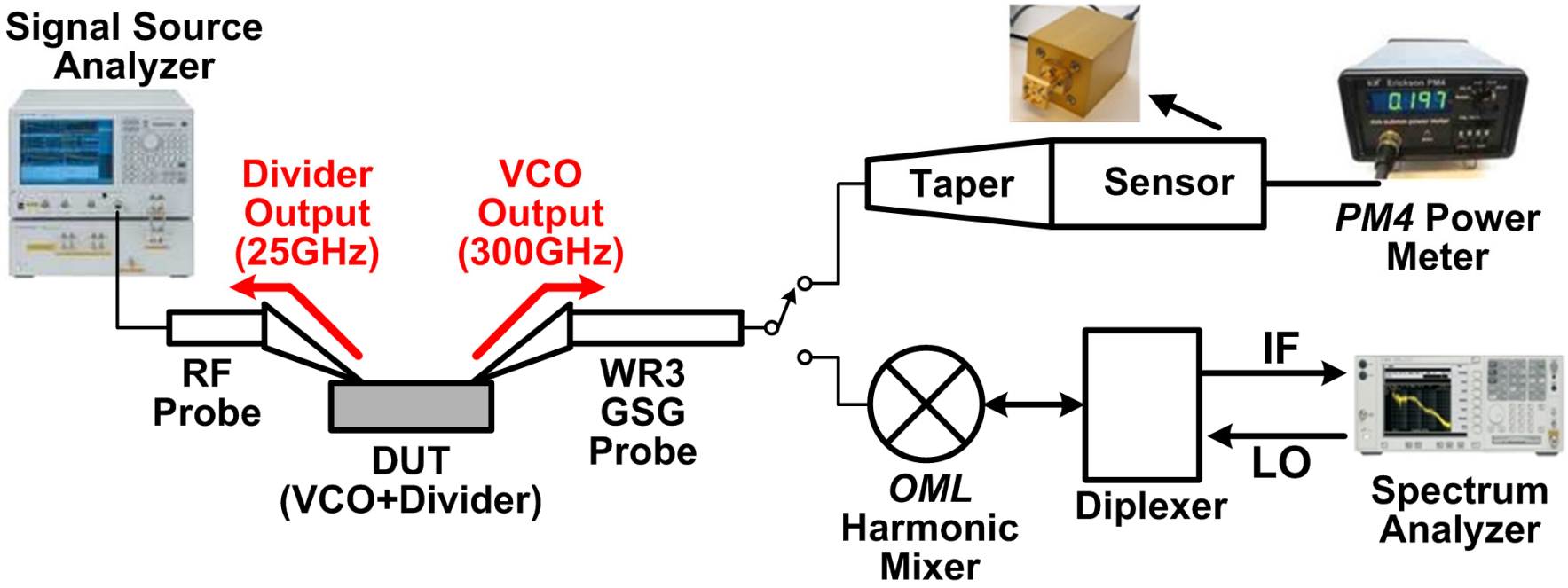
Measurement (Divider)





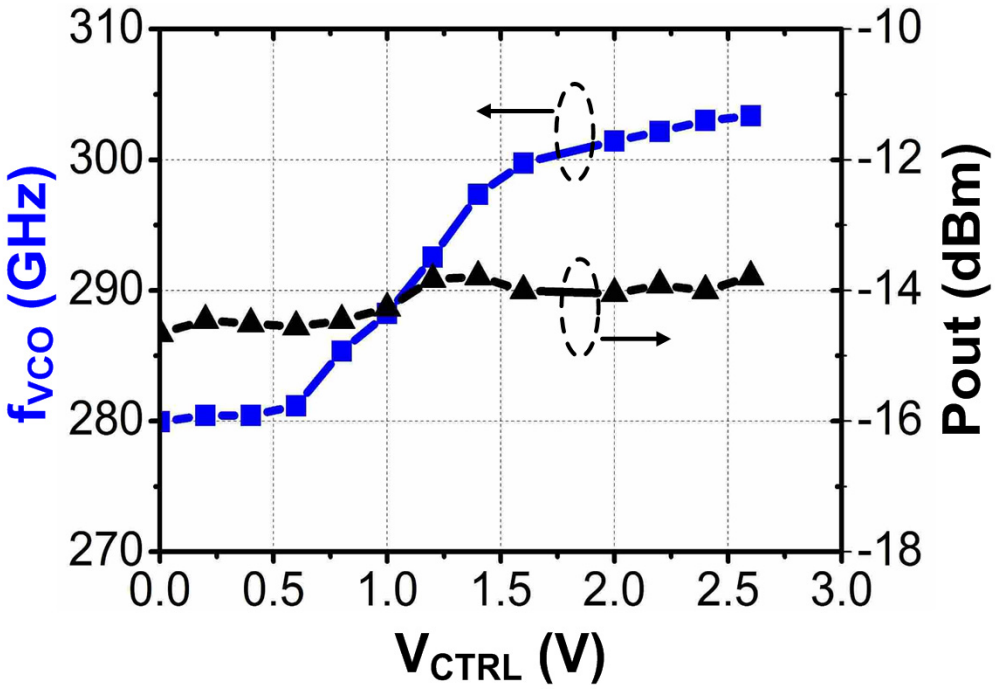
- The measured divider locking range is 93 ~ 101.8 GHz
- DC power consumption is 48.4 mW

Measurement (VCO+Divider)

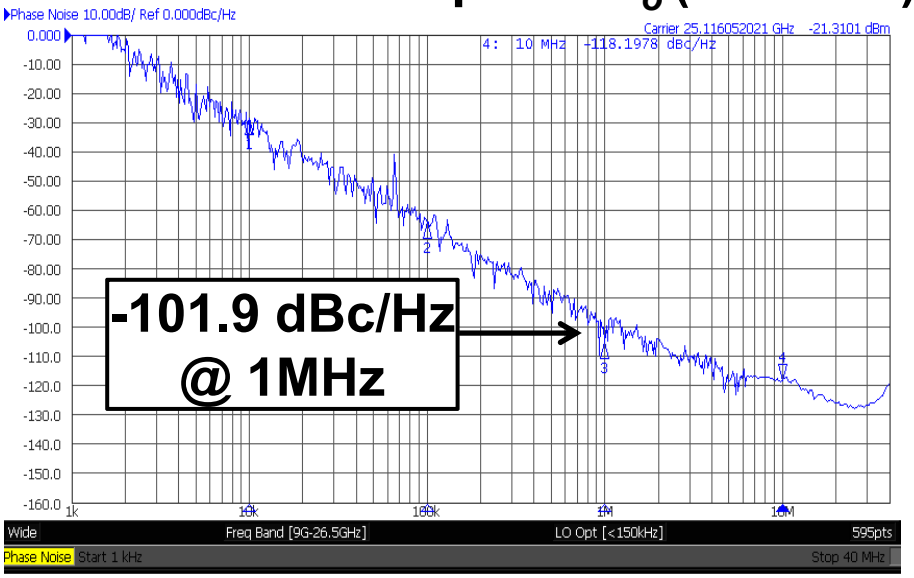


- The VCO output $3f_o$ is either fed to a power meter or down-converted to a spectrum analyzer
- The divider output $1/4f_o$ signal is used for phase noise measurement

Measurement Results (VCO)

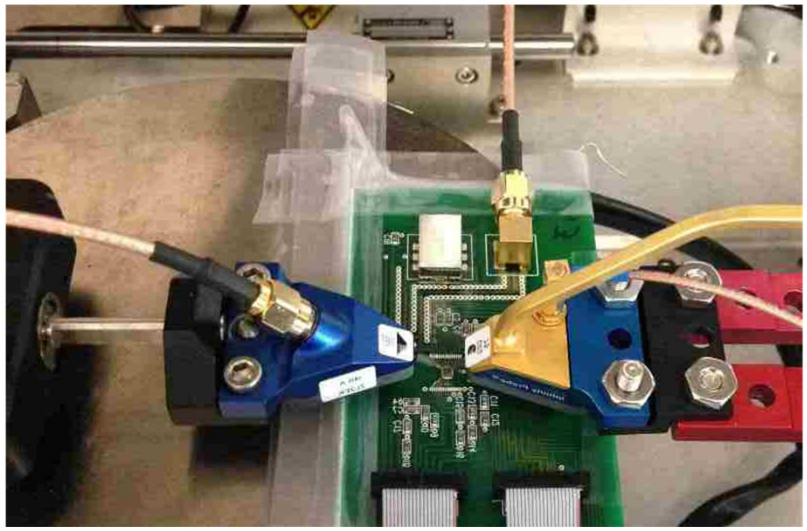


PN of Divider Output $1/4f_o$ (25.1GHz)



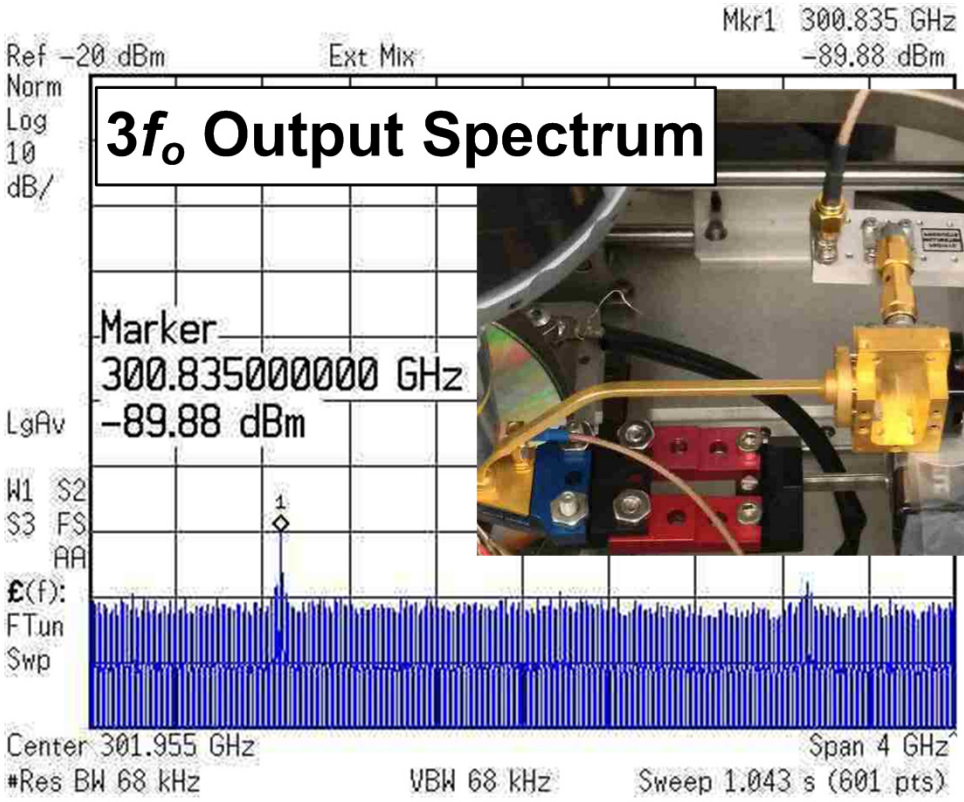
- The VCO achieves a tuning range of 280~303 GHz (8%) and an output power of –14 dBm
- The frequency-scaled VCO phase noise is –80.3 dBc/Hz @ 1 MHz offset (-101.9+20log12)

Close loop Measurement

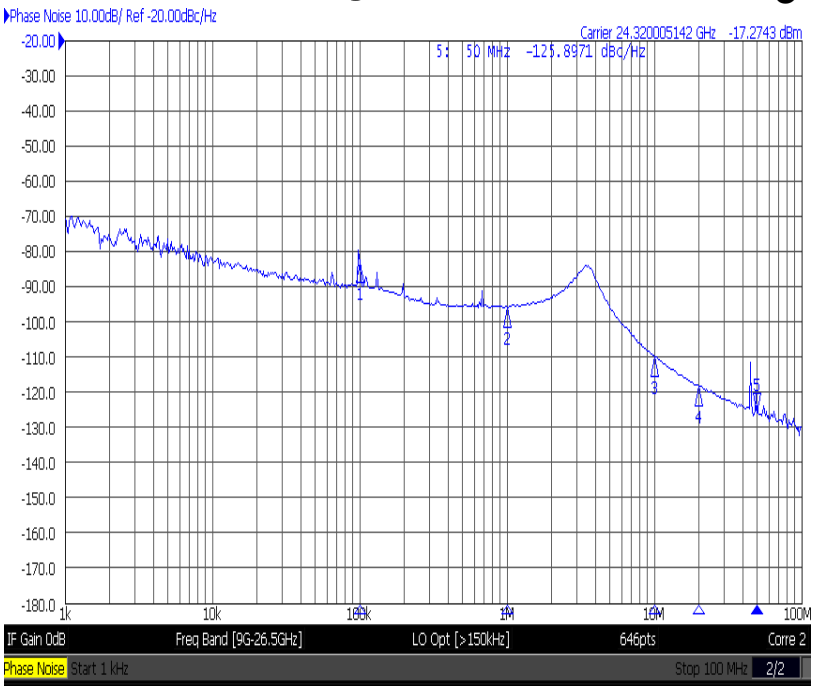


- The synthesizer input is fed to either a signal generator or crystal oscillator for its phase noise and locking range measurement
- Under a given input signal with the measured spectra of the 3f_o and 1/4f_o, the synthesizer close loop locking behavior can be observed

Measurement Results (Synthesizer)

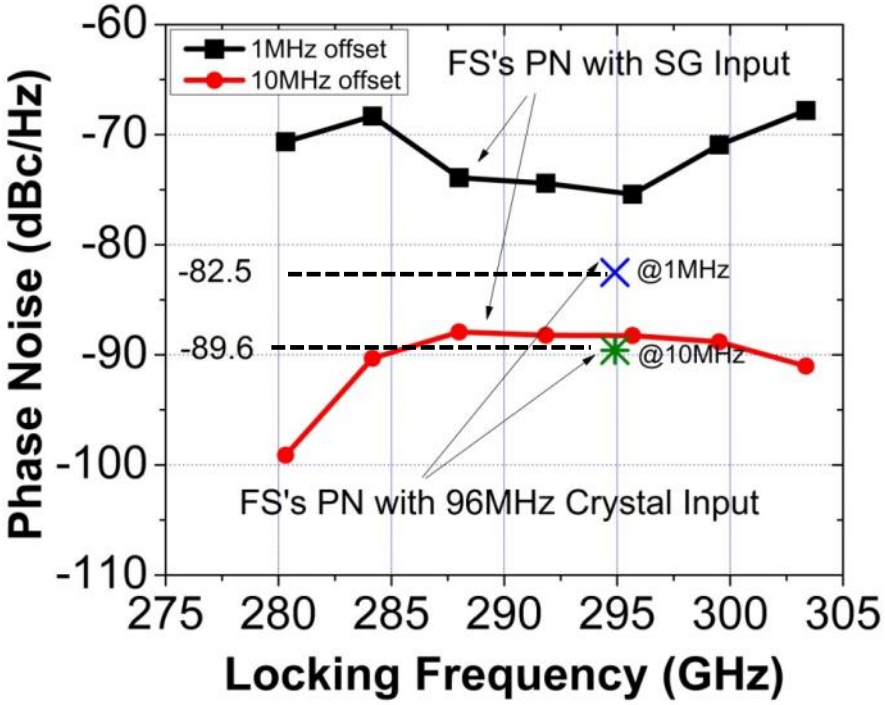


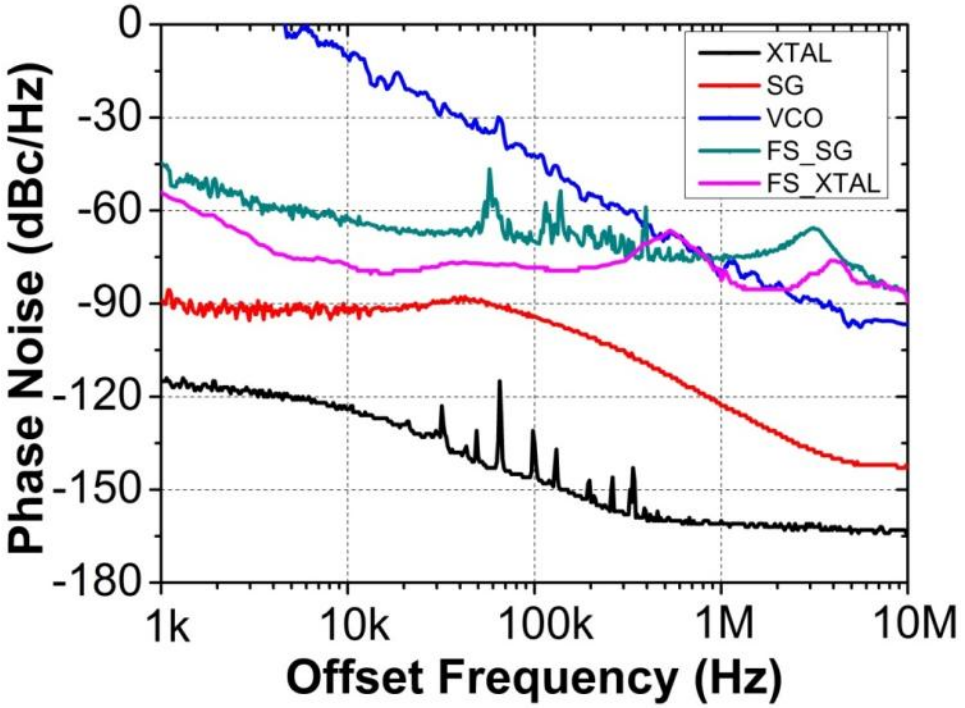
PN of the synthesizer 1/4f_o



- The 300.8 GHz signal is measured after down-conversion
- The synthesizer PN is obtained from the frequency-scaled PN of the 1/4f_o output
- The measured PN of the 1/4f_o (24.32 GHz)shows the synthesizer is locked to a 95 MHz reference input

Measurement Results (Synthesizer)





- The synthesizer achieves a locking range of 280~303 GHz
- With a signal generator (SG) as the input, the PN of 292 GHz is –74.4 dBc/Hz (–88.2 dBc/Hz) at 1 MHz (10 MHz) offset
- With a crystal oscillator as the input, the PN is –82.5 dBc/Hz (–89.6 dBc/Hz) at 1 MHz (10 MHz) offset

Performance Summary

Three-Phase Injection-Locked Divider		Triple-Push VCO		300GHz Frequency Synthesizer	
Frequency (GHz)	93 ~ 101.8	**Frequency (GHz)**	280 ~ 303.36	**Frequency (GHz)**	280.32 ~ 303.36
Divider Ratio	4	**Tuning Range**	8%	**Divider ratio**	1024
Locking Range	10.2%	**Output Power**	–14 dBm	**Locking Range**	7.9%
Input Power	< 0 dBm	**PN @ 1MHz offset (dBc/Hz)**	–80.28	**PN @ 100kHz offset (dBc/Hz)**	–77.8 @ 294.9GHz
Supply (V)	2	**Supply (V)**	1.8	**PN @ 1MHz offset (dBc/Hz)**	–82.5 @ 294.9GHz
DC Power	48.4 mW	**DC Power**	105.6 mW	**DC Power**	376 mW

Comparison Table

	This work	*MTT-S* 2011 [3]	*JSSC* 2011 [2]
Frequency (GHz)	280.32 ~ 303.36 (3rd)	300.76 ~ 301.12 (fund.)	160 ~ 169 (2nd)
Divider ratio	1024	10	128
Locking Range	7.9%	0.12%	5.5%
PN @ 100kHz/1MHz offset (dBc/Hz)	–77.8 / –82.5 @ 294.9 GHz	–78 / –85 @ 300.96 GHz	–75 / –78 @ 163 GHz
DC Power (P_D)	376 mW	301.6 mW	1250 mW
FOM_T^* @ 100kHz/1MHz offset	–179.4 / –163.9 dBc/Hz	–144.4 / –131.36 dBc/Hz	–163.1 / –146.1 dBc/Hz
Technology (f_{max})	90nm SiGe BiCMOS (315 GHz)	InP HBT (800 GHz)	130nm SiGe BiCMOS (280 GHz)

$$* FOM_T = PN - 20\log\left(\frac{f_o}{\Delta f}\cdot\frac{Locking\,Range}{10}\right) + 10\log\left(\frac{P_D}{1mW}\right)$$

Conclusion

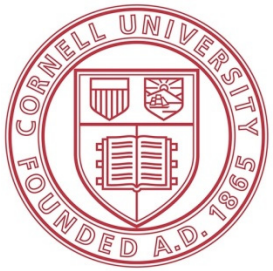
- A wide locking-range 300 GHz frequency synthesizer is presented
- The proposed CAV frequency-tunes and buffers the triple-push VCO with the minimum loading effect
- The proposed three-phase injection locked divider achieves wider BW at high frequency
- The similar structure of the VCO and divider allows for a compact layout and circuit co-design
- The synthesizer demonstrates the highest operation frequency and figure-of-merit among all the other silicon-based prior work

Acknowledgements

- *TowerJazz Semiconductor* for chip fabrication
- National Science Foundation (NSF)
- Professor Afshari from Cornell and *Agilent* for providing test equipments
- Sonnet Software and Cadence for design software
- NCIC members, especially Francis Caster and Dr. C.-C. Wang for technical discussion and support

A 247-to-263.5 GHz VCO with 2.6mW Peak Output Power and 1.14% DC-to-RF Efficiency in 65nm Bulk CMOS

Muhammad Adnan and Ehsan Afshari



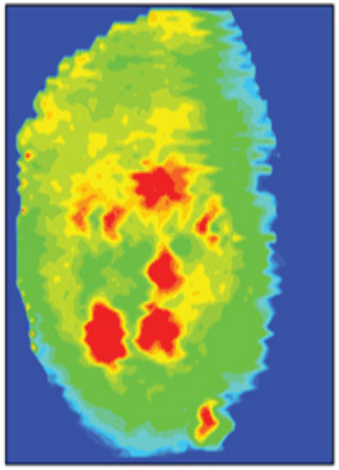
Ultra-high-speed Nonlinear IC (UNIC) Lab
Dept. of Electrical and Computer Engineering
Cornell University, Ithaca, NY

Outline

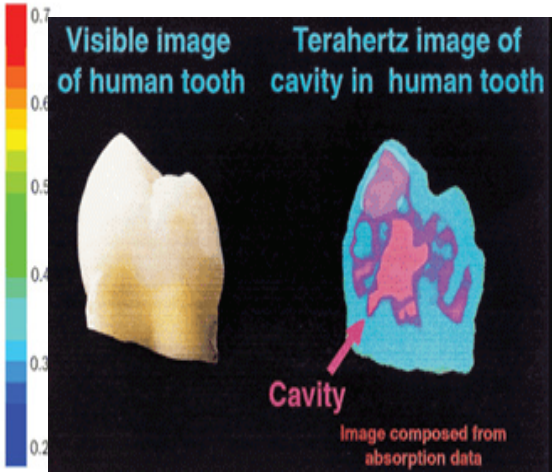
- **Motivation**
- **A Scalable THz VCO Architecture**
- **A Source-degenerated Self-feeding VCO**
- **Passive Coupling & Harmonic Extraction**
- **Design & Measurement of 2-stage VCO**
- **Design & Measurement of 8-stage VCO**
- **Conclusion**

Motivation

- Interesting applications from 100GHz to 10THz
- mm-wave and THz applications include
  - Spectroscopy and non-invasive imaging
  - Security (detection of concealed weapon & explosives)
  - High data-rate communication
- Need a *tunable, high power* signal source.

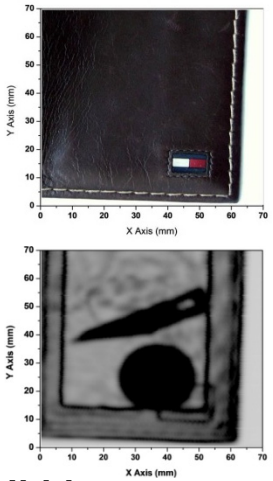


Skin tumor (red)



Tooth Cavity

Concealed weapon

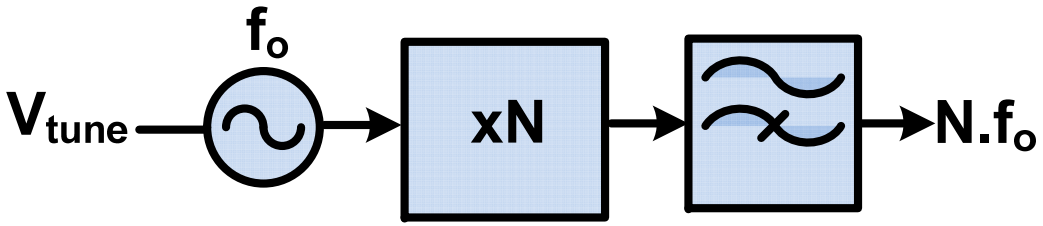


Hidden weapon

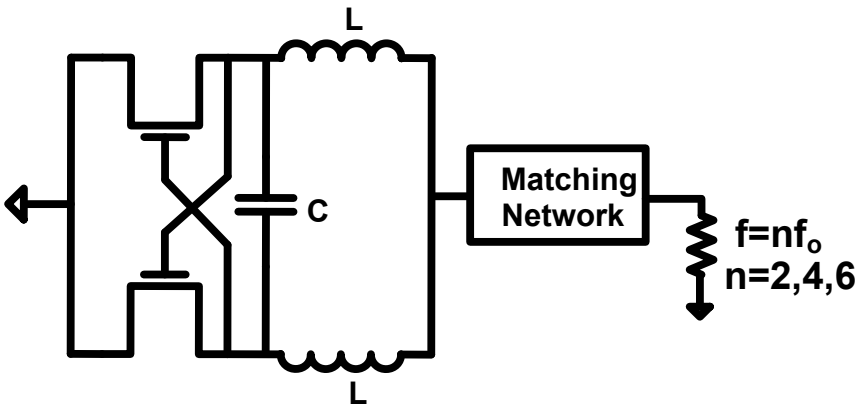
Courtesy R. Han

THz Signal Generation

- Frequency multipliers
  - Higher 3dB BW
  - High conversion loss

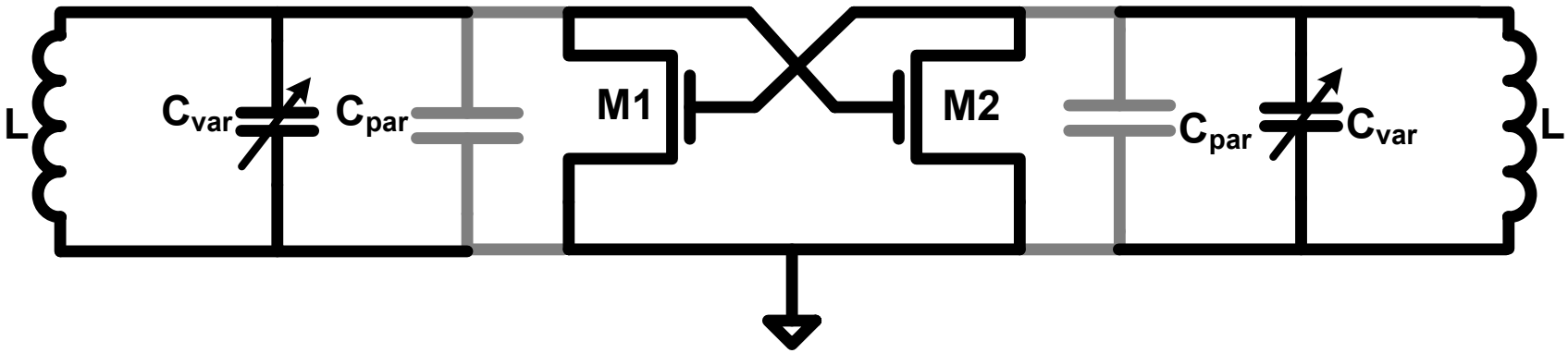


- Harmonic VCO
  - Integrated solution
  - Lower tuning range
  - Output power fluctuation
  - DC-to-THz efficiency < 0.5%



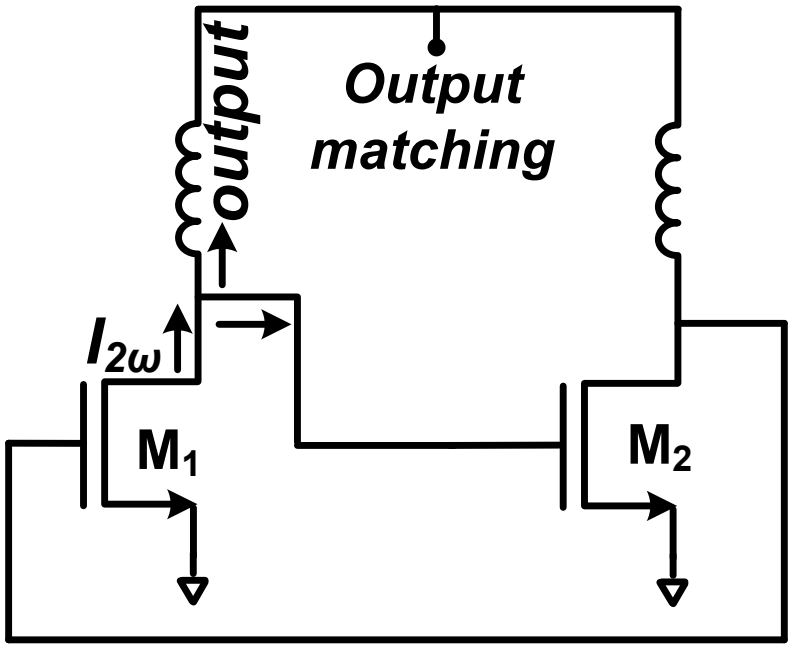
Challenges at Fundamental Freq.

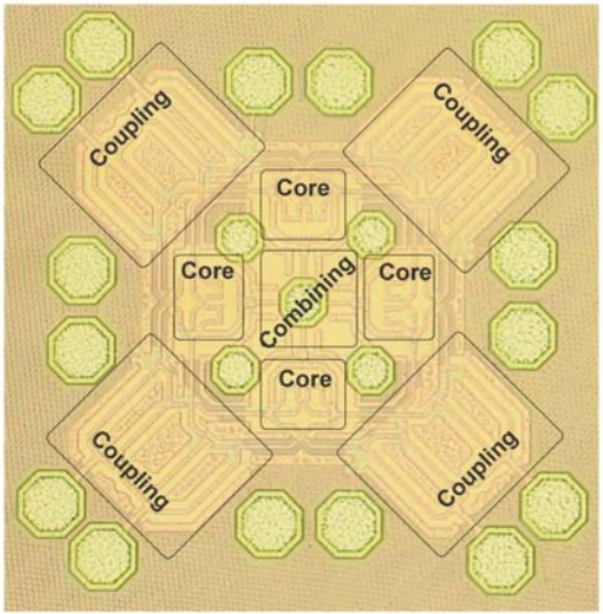
- **High power:**
  - Loss of varactors
    - Q<10 at ~100GHz in a standard CMOS
- **High tunability not easy with varactor**
  - Device parasitic
    - The varactor size is comparable to the parasitics



Challenges at Harmonics

- Harmonic efficiency
  - Undesired leakage of harmonic current
  - Output power combining ~ layout challenges
- Effective suppression of undesired mode





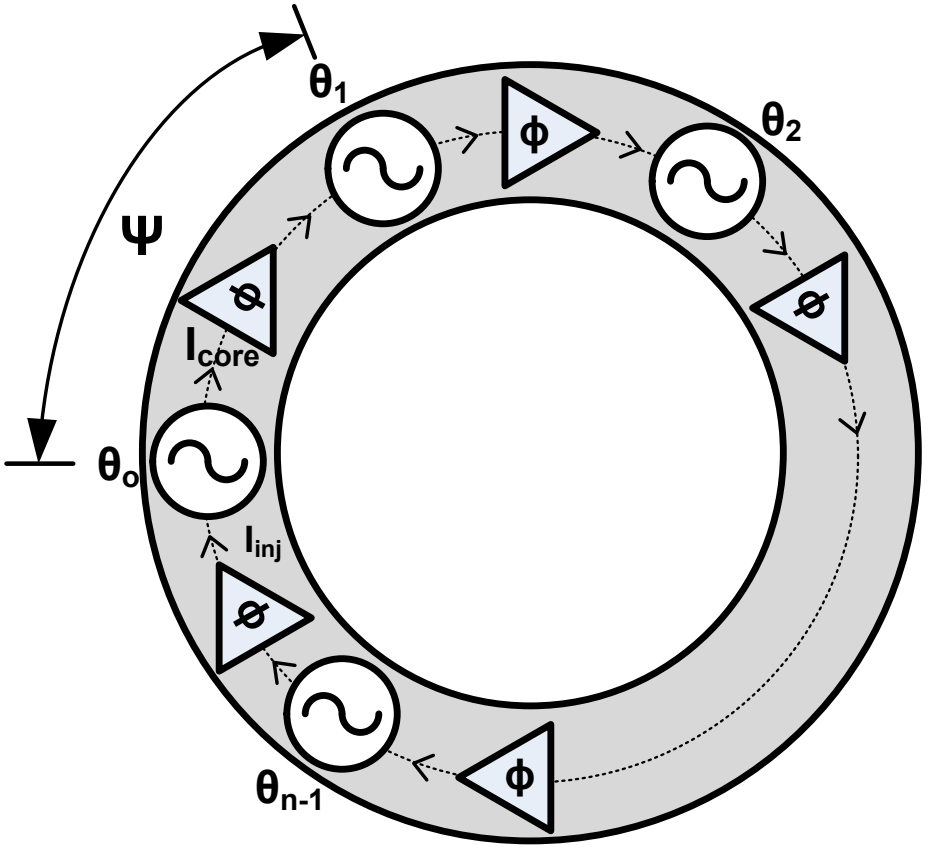
Y. Tousi, etc. – ISSCC 2012

Outline

- Motivation
- A Scalable THz VCO Architecture
- A Source-degenerated Self-feeding VCO
- Passive Coupling & Harmonic Extraction
- Design & Measurement of 2-stage VCO
- Design of 8-stage VCO
- Conclusion

THz VCO Architecture

- **Unidirectionally coupled oscillators:**
  - **Generate high power**
  - **Better phase noise**



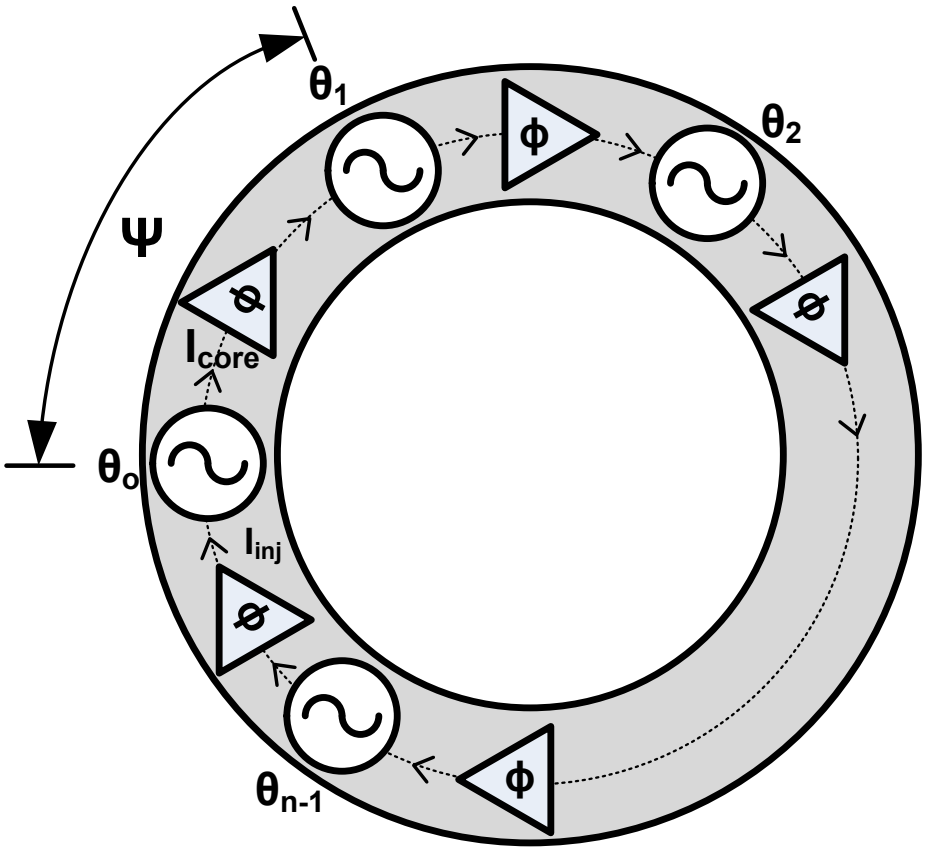
THz VCO Architecture

- **Unidirectionally coupled oscillators:**
  - **Generate high power**
  - **Better phase noise**
- **Tuning:**
  - **Capacitive tuning**

$$\frac{\Delta\omega_c}{\omega_o} = \frac{\Delta C}{2C_o}$$

  - **Delay-based tuning**

$$\sum_i \psi_i = 2k\pi$$



THz VCO Architecture

- **Tuning mechanisms:**
  - **Capacitive tuning**

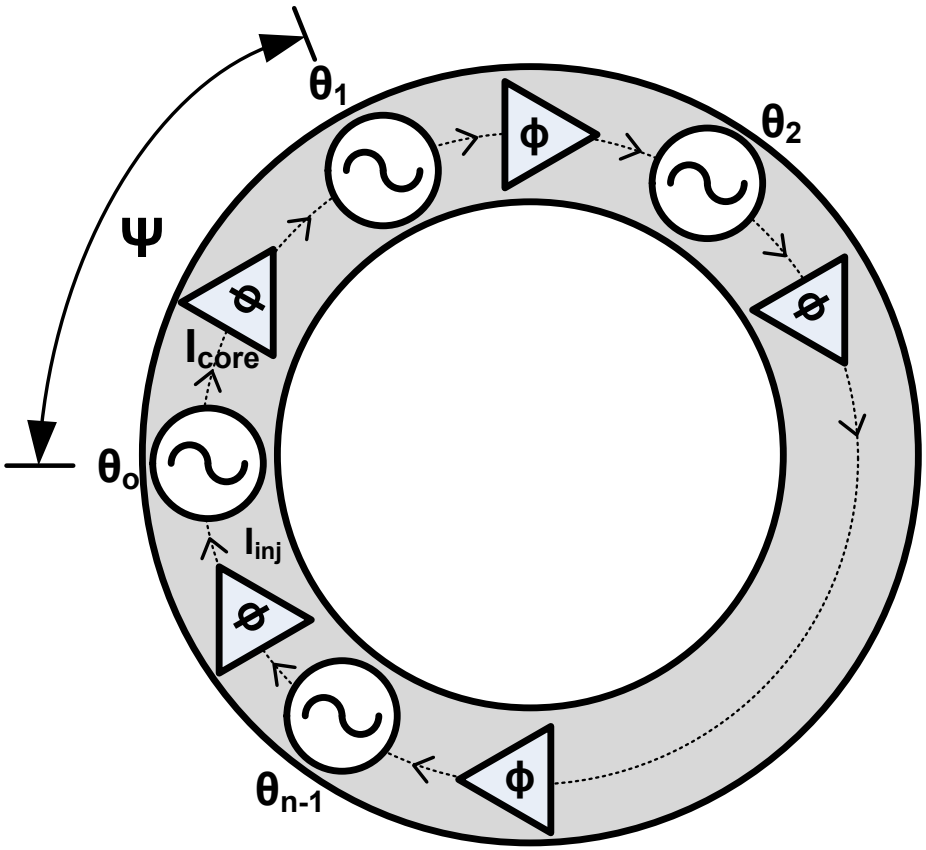
$$\frac{\Delta\omega_c}{\omega_o} = \frac{\Delta C}{2C_o}$$

  - **Delay-based tuning**

$$\Delta\theta = \theta_i - \theta_{i-1} - \phi$$

$$\frac{\Delta\omega_d}{\omega_o} = K.sin(\Delta\theta)$$

$$K = \frac{I_{inj}}{I_{core}}\frac{\omega_o}{2Q}$$



THz VCO Architecture

- **Tuning mechanisms:**
  - **Capacitive tuning**

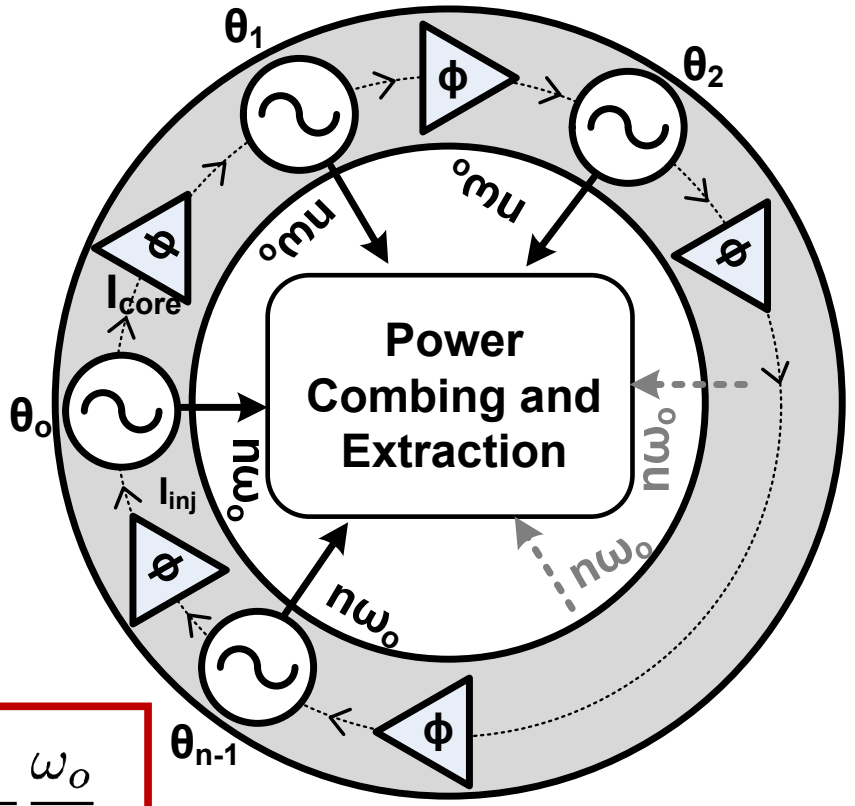
$$\frac{\Delta\omega_c}{\omega_o} = \frac{\Delta C}{2C_o}$$

  - **Delay-based tuning**

$$\frac{\Delta\omega_d}{\omega_o} = K.sin(\Delta\theta)$$

  - **Total tuning range**

$$\frac{\Delta\omega_{max}}{\omega_o} = \frac{\Delta C_{max}}{C_o} + \frac{I_{inj}}{I_{core}}\frac{\omega_o}{Q}$$

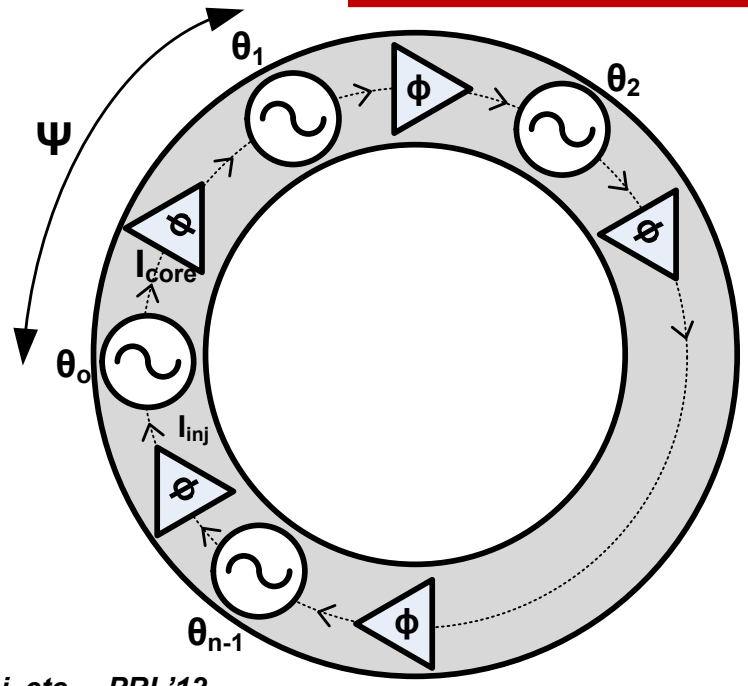


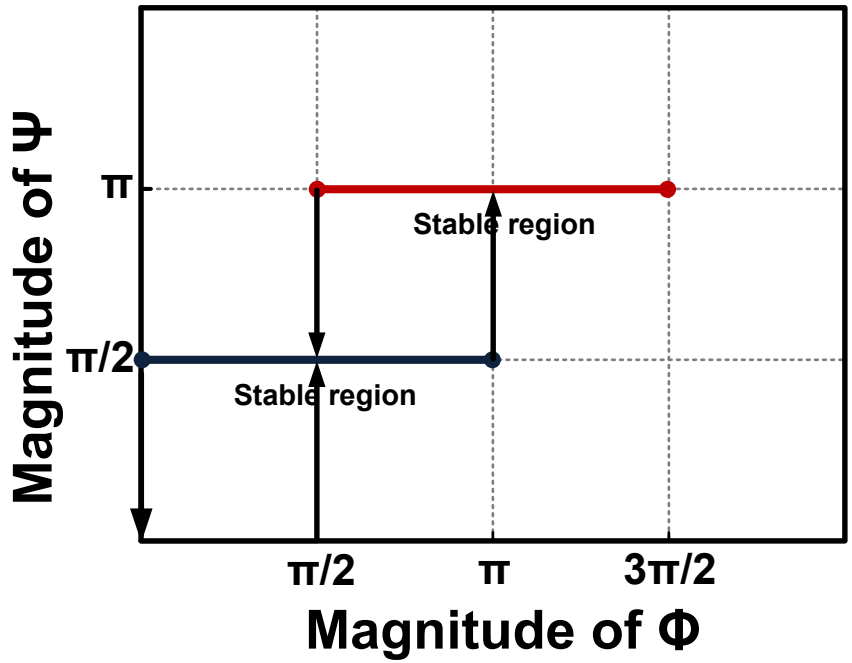
Stability Analysis

- **Perturbation analysis yields following stability condition:**

$$K_s = (1 + \frac{\Delta C}{C_o}) \frac{I_{inj}}{I_{core}} \frac{\omega_o}{2Q} \geq 0$$

$$\psi + \pi/2 \geq \phi \geq \psi - \pi/2$$





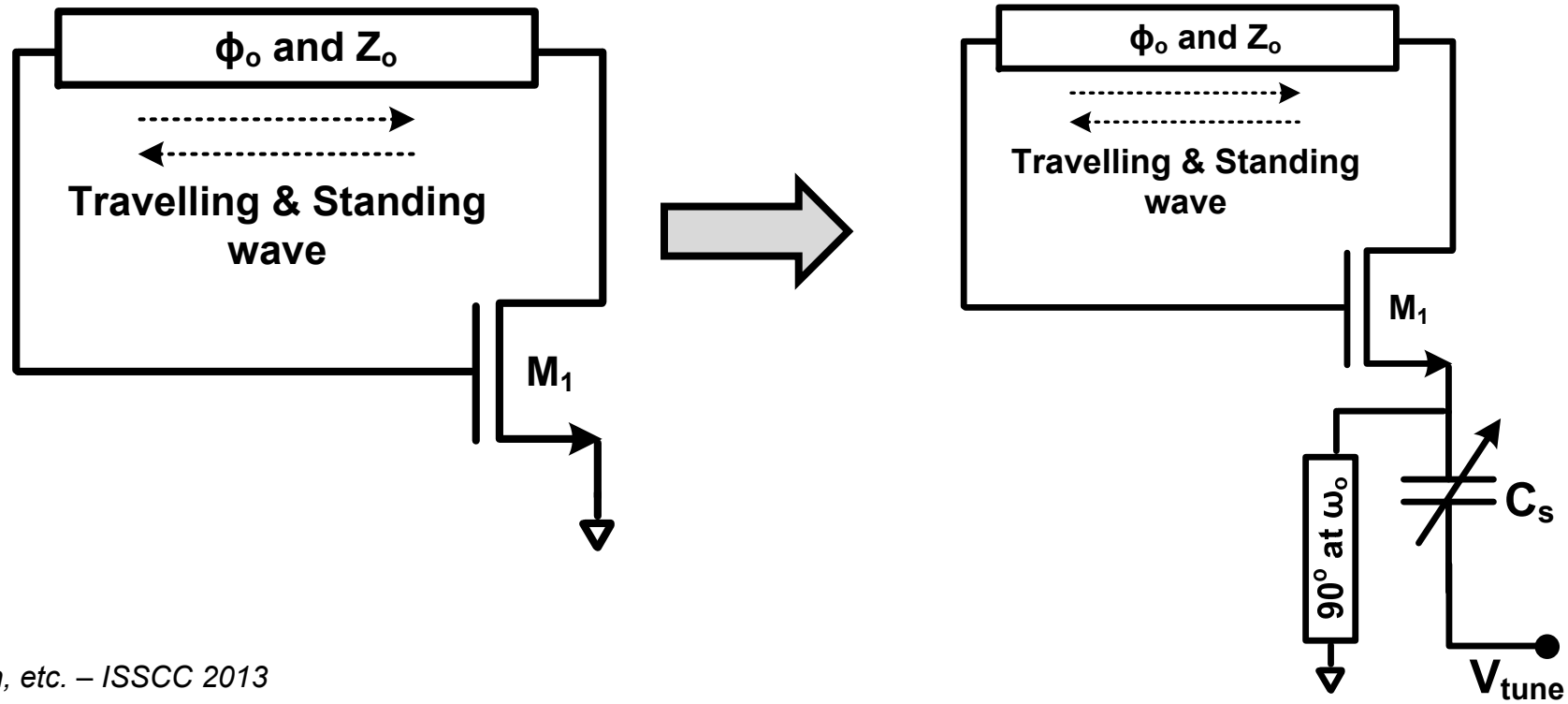
Y. Tousi, etc. – PRL'12

Outline

- Motivation
- A Scalable THz VCO Architecture
- A Source-degenerated Self-feeding VCO
- Passive Coupling & Harmonic Extraction
- Design & Measurement of 2-stage VCO
- Design of 8-stage VCO
- Conclusion

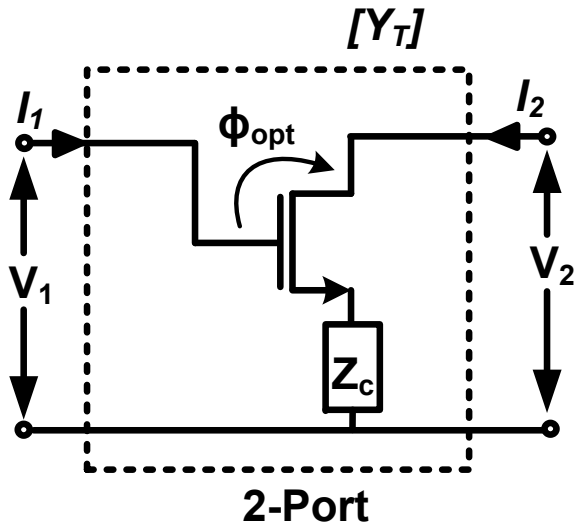
Source-degenerated Self-feeding VCO

- Each core is implemented as modified self feeding VCO.
- Source degeneration provides
  - Capacitive tuning
  - Coupling phase delay



R. Han, etc. – ISSCC 2013

Optimizing for Maximum Power



- If g_{ij} and b_{ij} are real and imaginary part of Y_{Tij} then

$$P_{out} = -g_{11}|V_1|^2 - g_{22}|V_2|^2 - |V_1||V_2|\left((g_{12}+g_{21})cos\angle A - (b_{21}-b_{12})sin\angle A\right)$$

- In oscillator:

$$|A| = 1$$

- Optimum phase of A can be calculated as

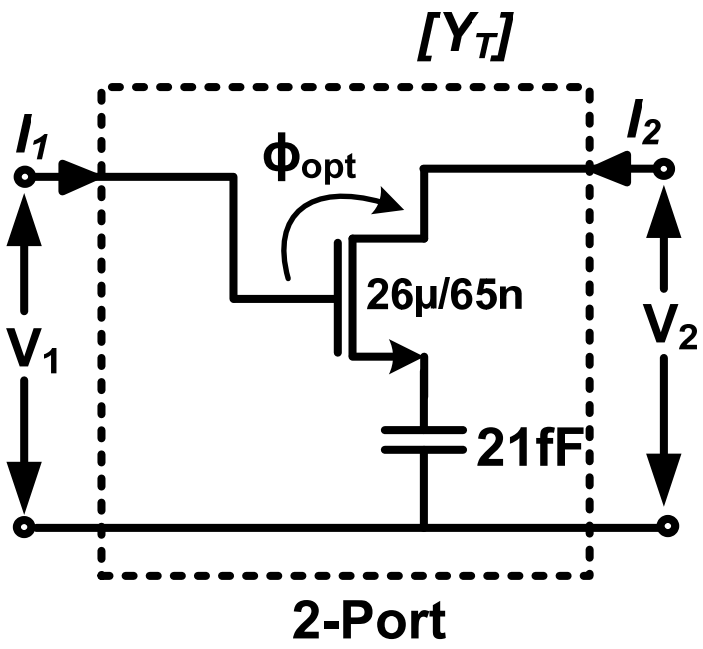
$$\angle A_{opt} = \phi_{opt} = \angle - (Y_{T21} + Y_{T12}^*)$$

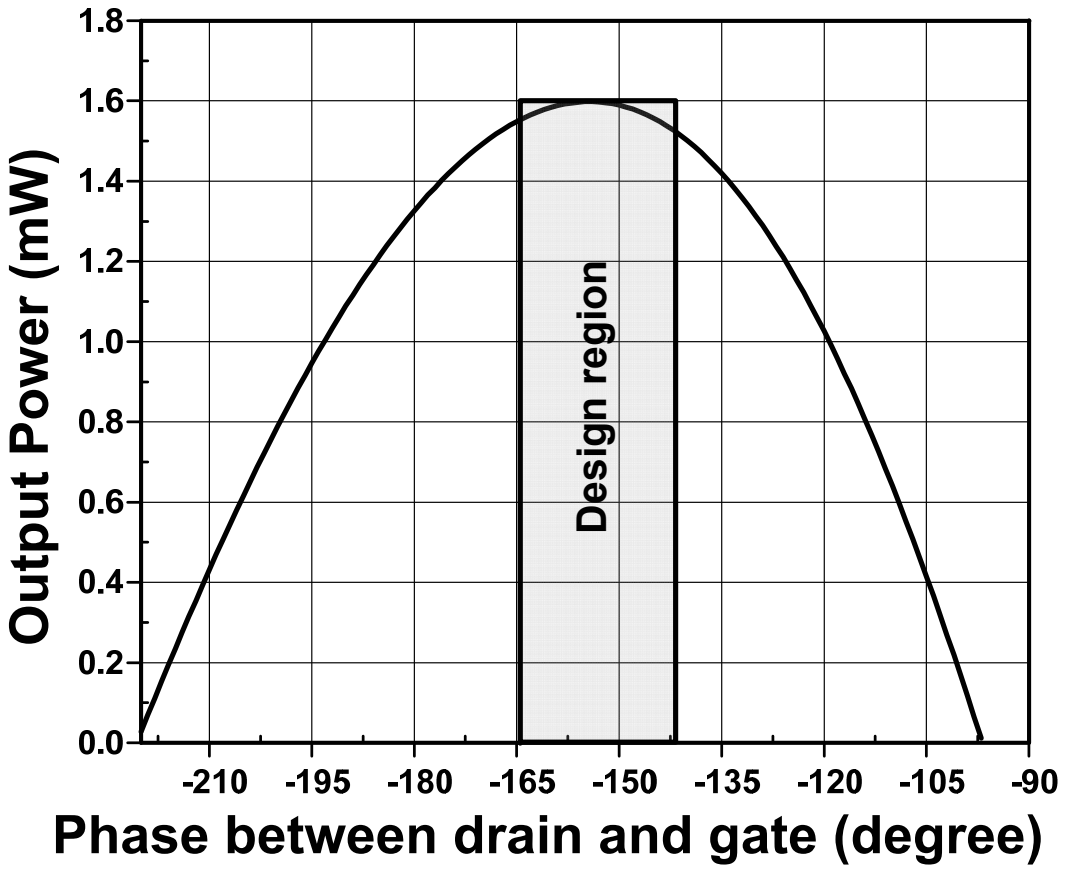
O. Momeni, etc. – JSSC 2011

Optimizing for Maximum Power

- **Net power maximum at optimum phase**

$$\angle A_{opt} = \phi_{opt} = \angle - (Y_{T21} + Y_{T12}^{*})$$



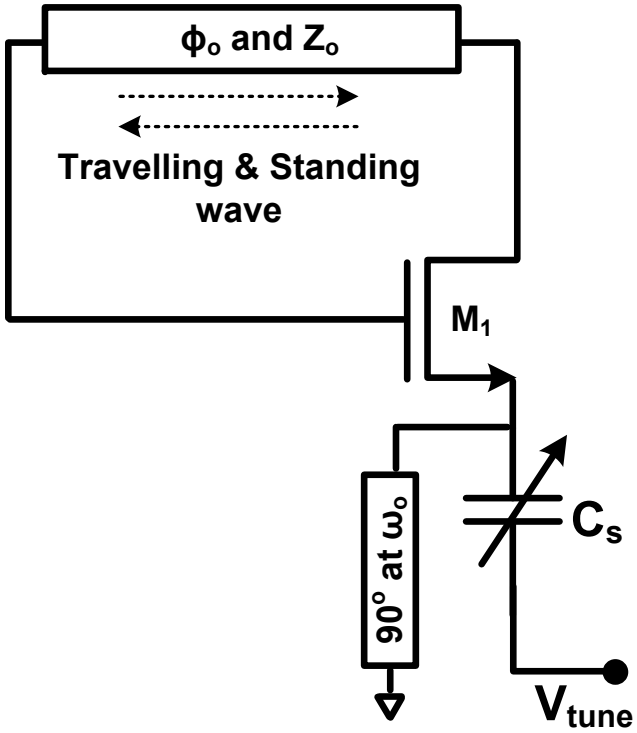


Source-degenerated Self-feeding VCO

- Gate-drain transmission line helps to achieve optimum phase shift
- The exact mathematical expression is

$$Z_o sin(\phi_o) = \frac{Im(A_{opt})}{g_{11} + Re(A_{opt}.Y_{T12})}.$$

- Different sets of (Z_0, φ_{TL}) achieve the optimum phase at 125GHz
- For example Z_0=58Ω , φ_{TL}=69 for Cs = 20fF satisfy the above relation

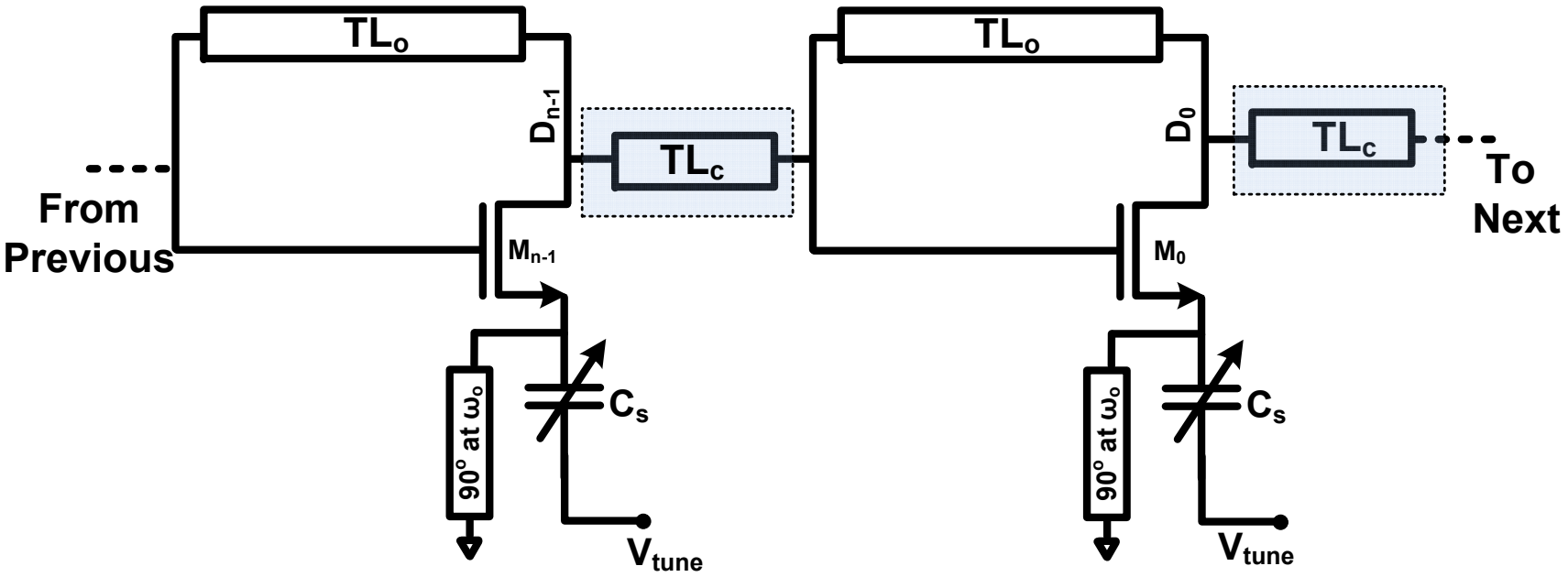


Outline

- Motivation
- A Scalable THz VCO Architecture
- A Source-degenerated Self-feeding VCO
- Passive Coupling & Harmonic Extraction
- Design & Measurement of 2-stage VCO
- Design of 8-stage VCO
- Conclusion

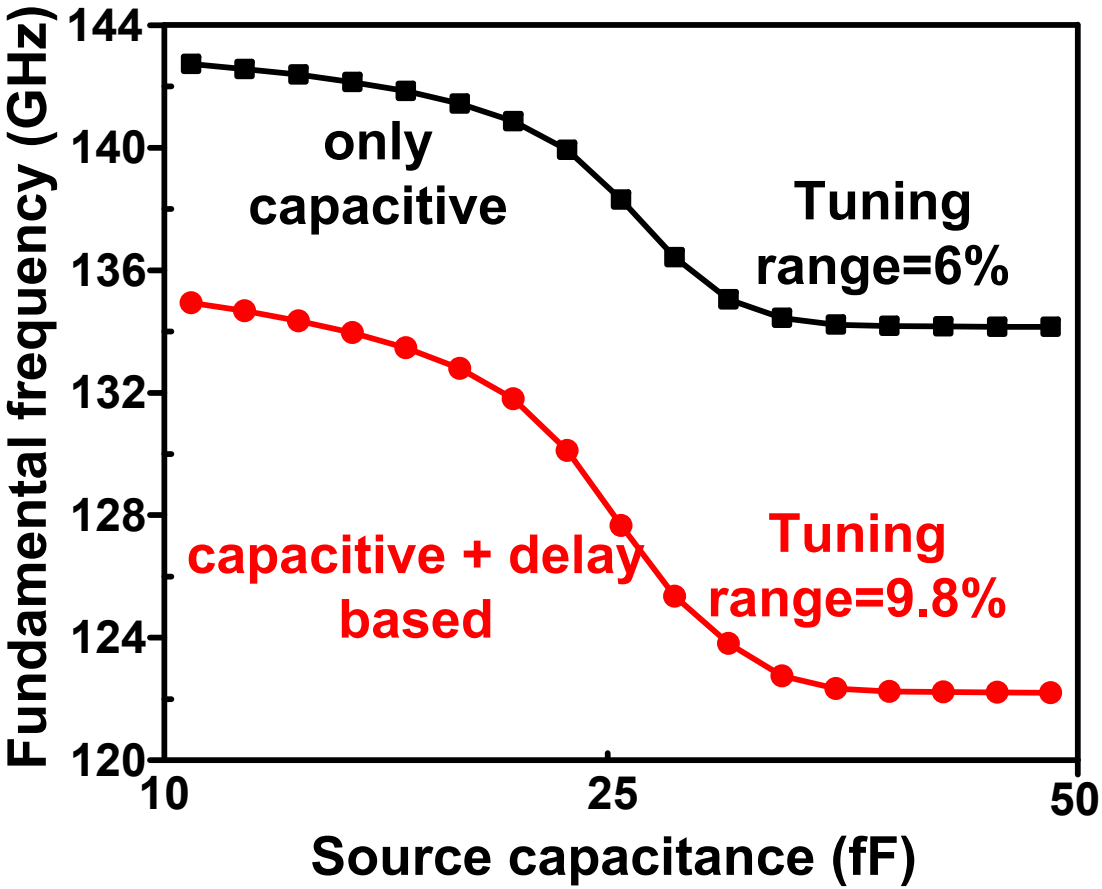
Coupling and Harmonic Extraction

- Passive coupling is employed
- Varactor performs both
  - Capacitive tuning
  - Delay based tuning



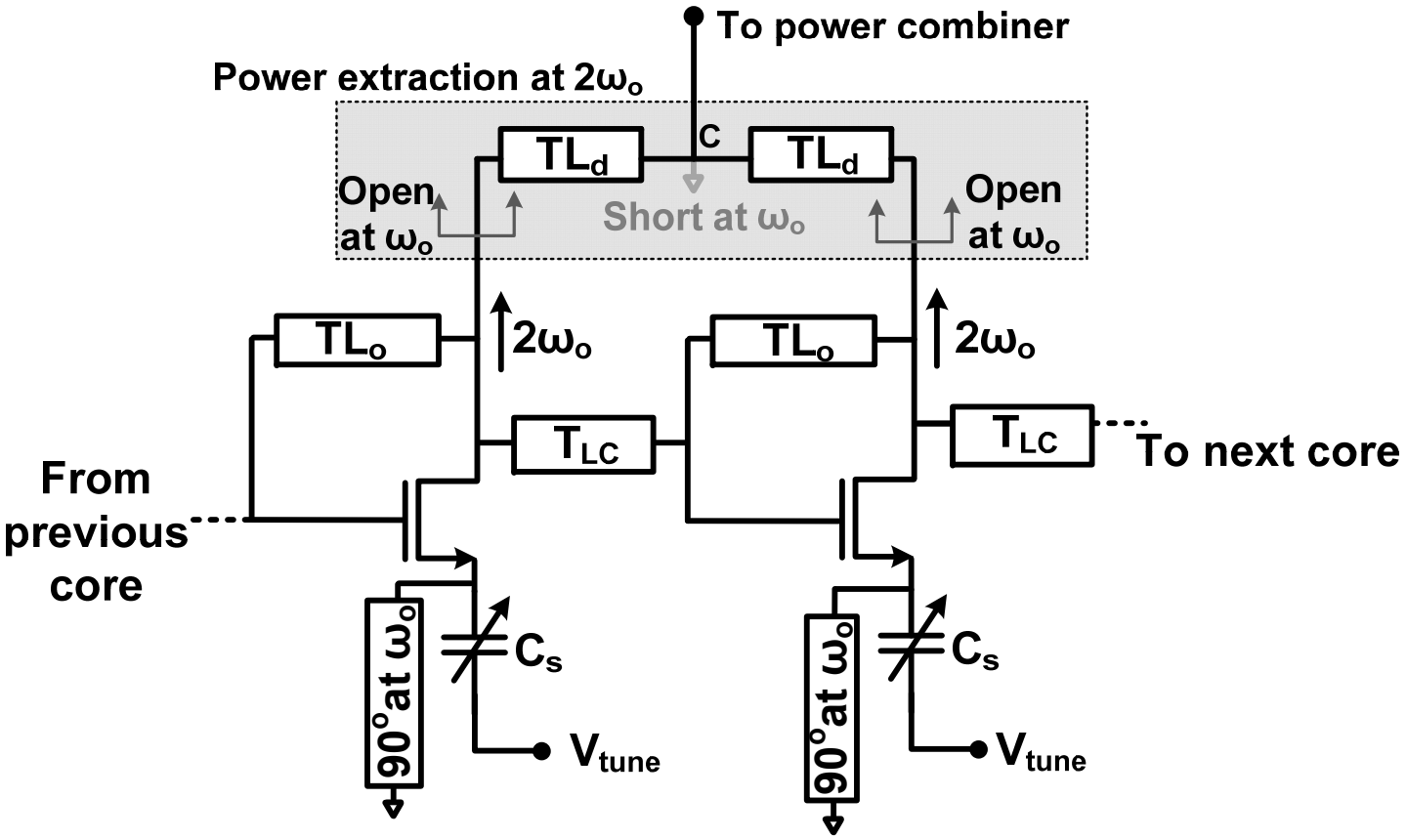
Closed Loop vs. Open Loop Tuning

- Simulation of 2-stage VCO
- Capacitive + delay based tuning enhanced tuning range



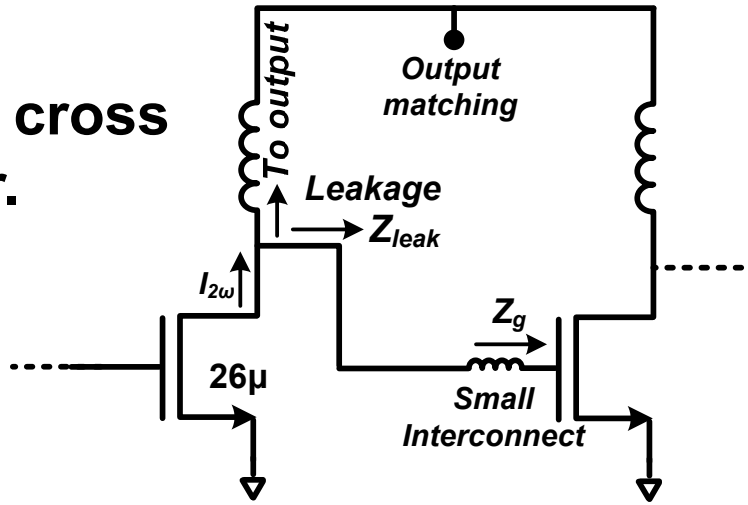
Harmonic Extraction

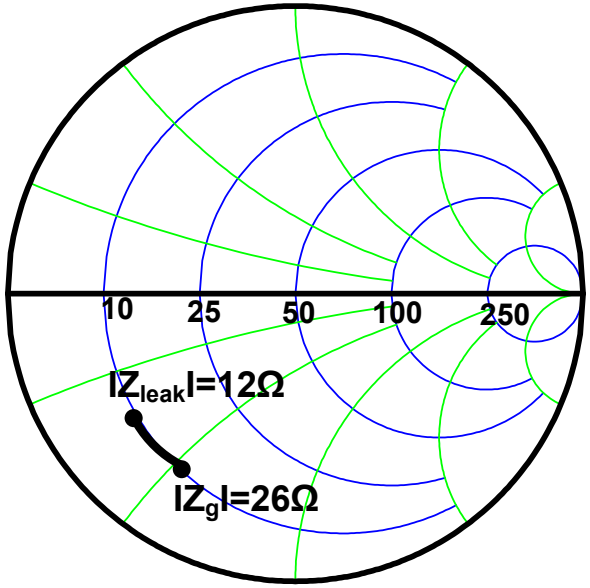
- 2nd harmonic is extracted
- Harmonic extraction is invisible to fundamental differential operation



Harmonic Extraction Efficiency

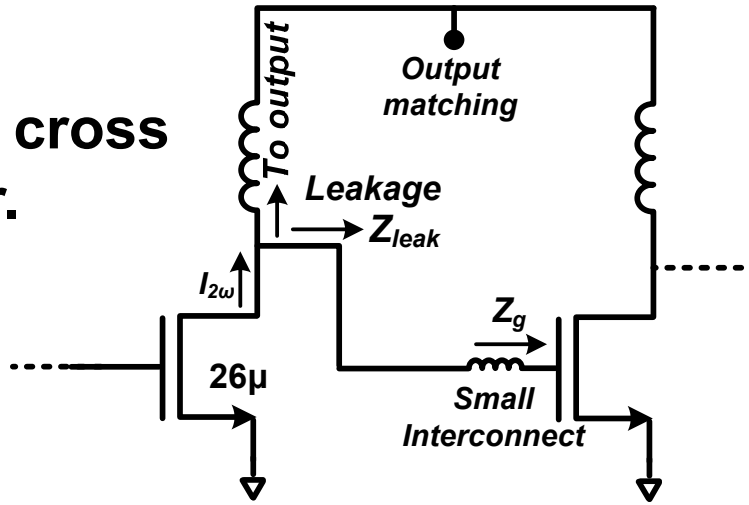
- **Standard ring or cross coupled oscillator.**

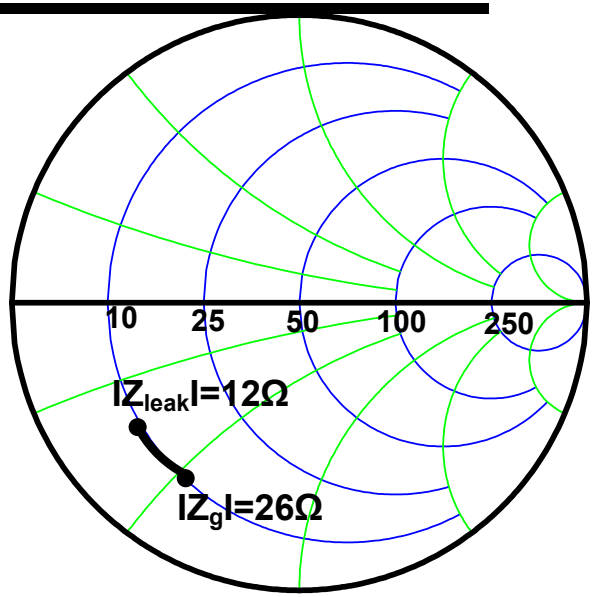




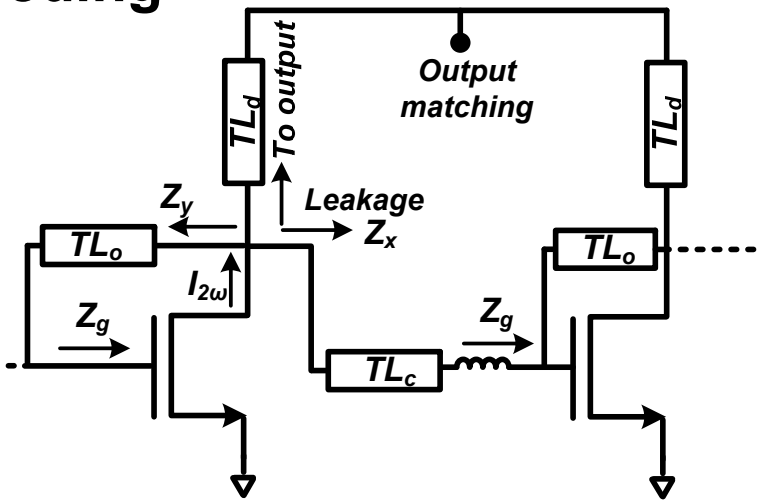
Harmonic Extraction Efficiency

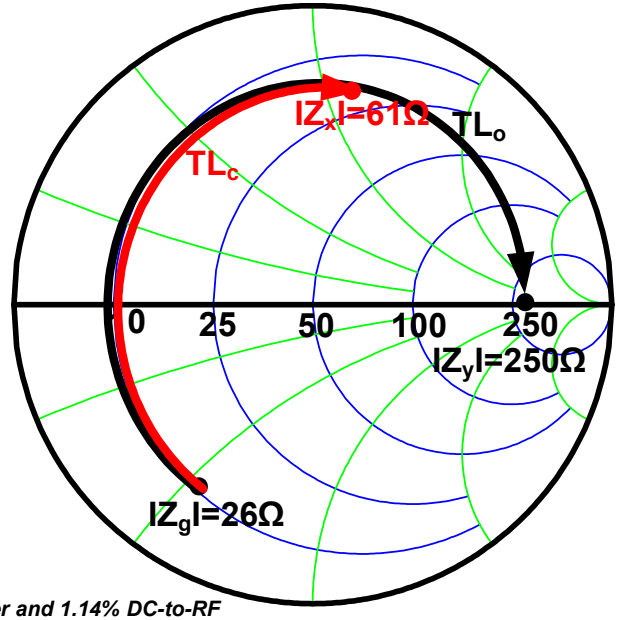
- **Standard ring or cross coupled oscillator.**





- **Modified self-feeding at 2nd harmonic**



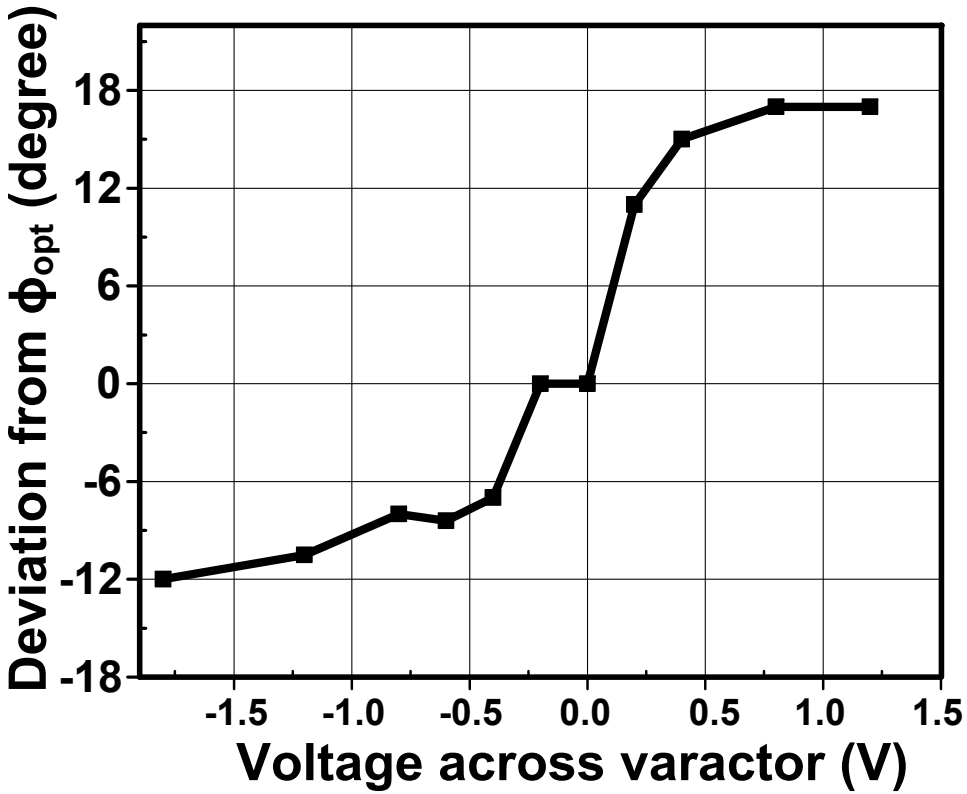


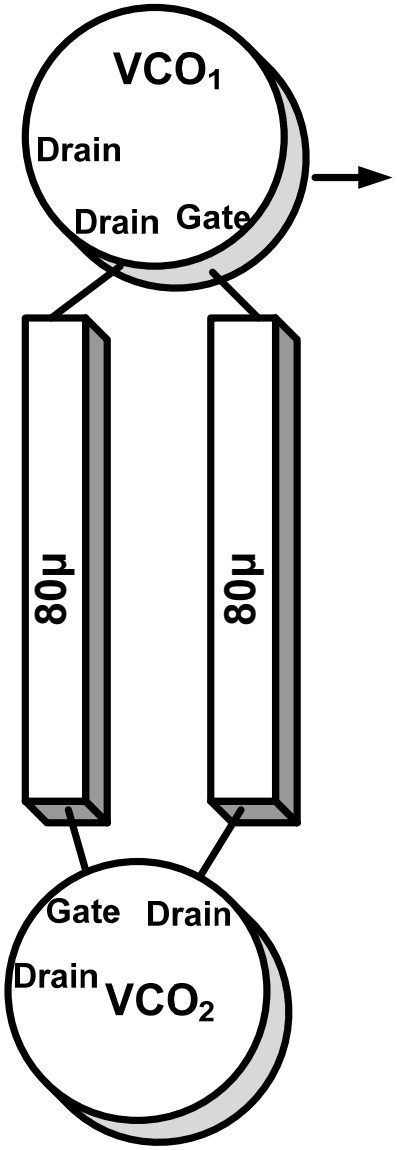
Outline

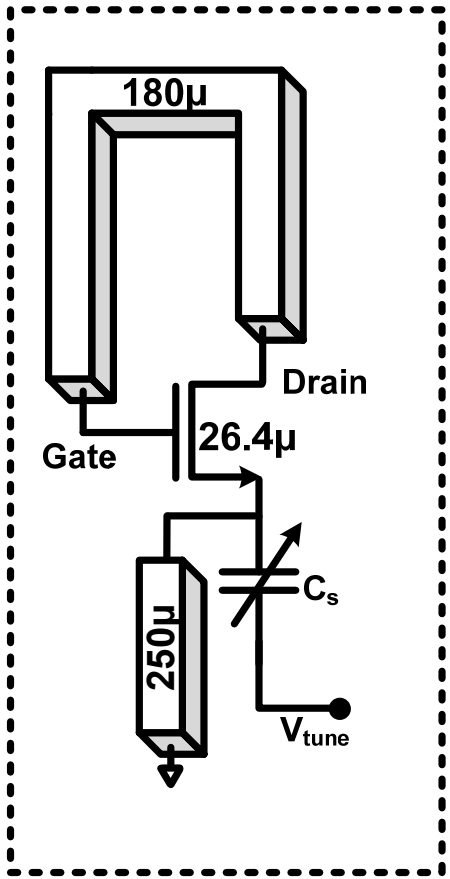
- Motivation
- A Scalable THz VCO Architecture
- A Source-degenerated Self-feeding VCO
- Passive Coupling & Harmonic Extraction
- Design of 2-stage VCO
- Design of 8-stage VCO
- Conclusion

2-Stage VCO Prototype

- Schematic of 2-stage VCO

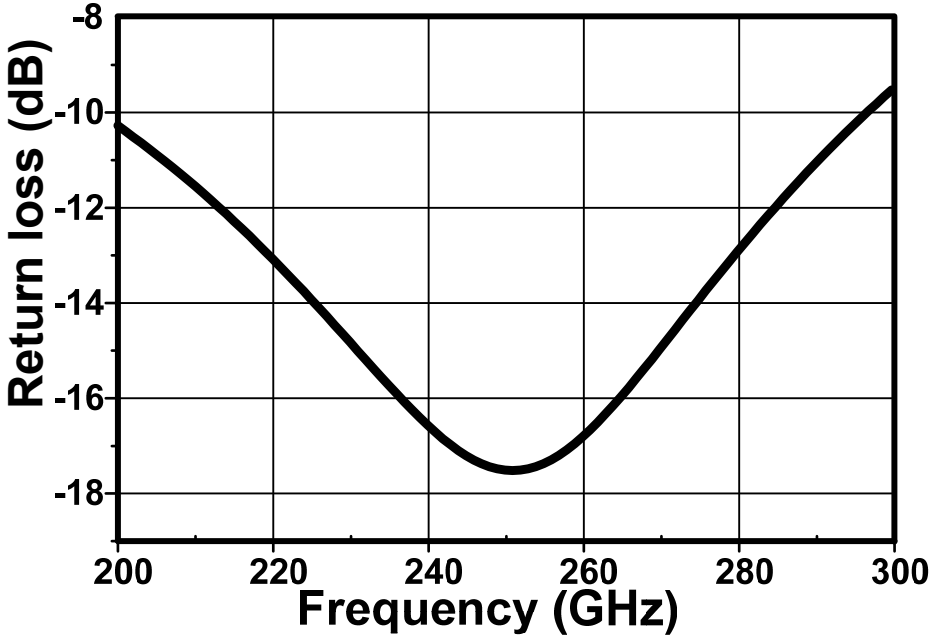


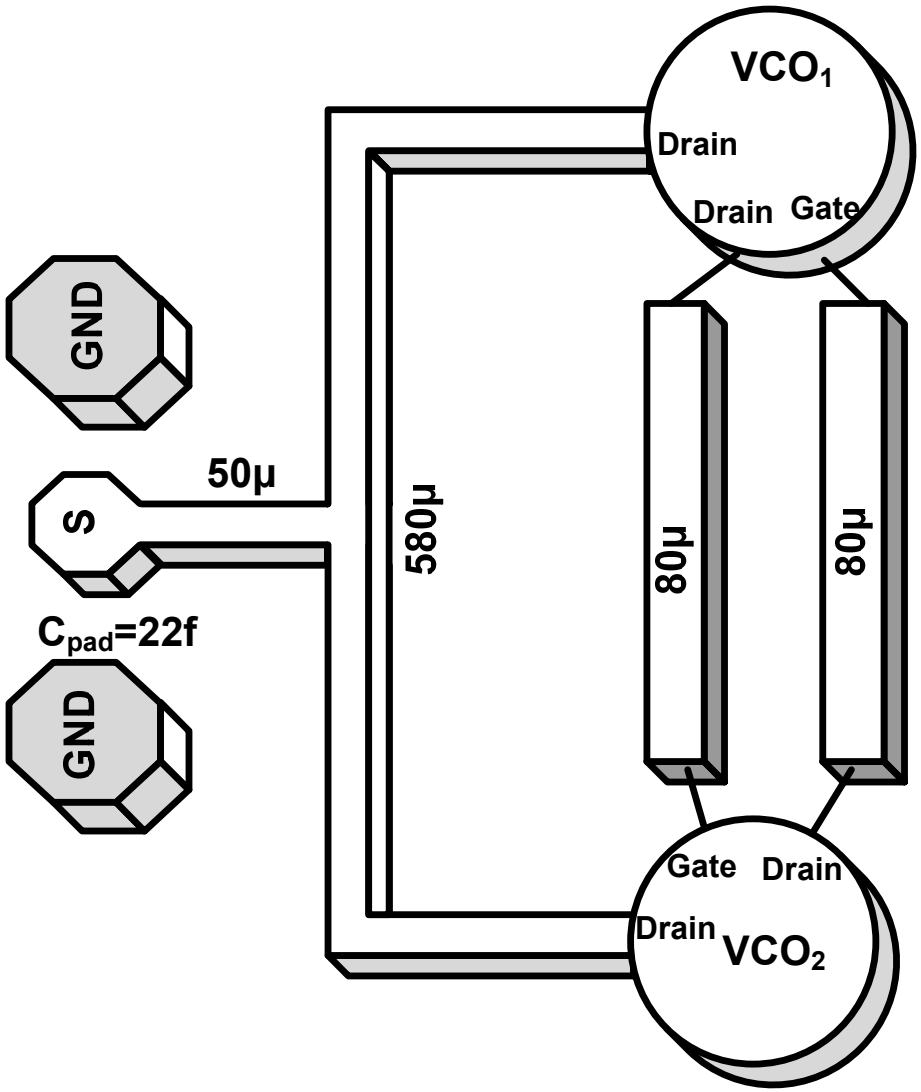




2-Stage VCO Prototype

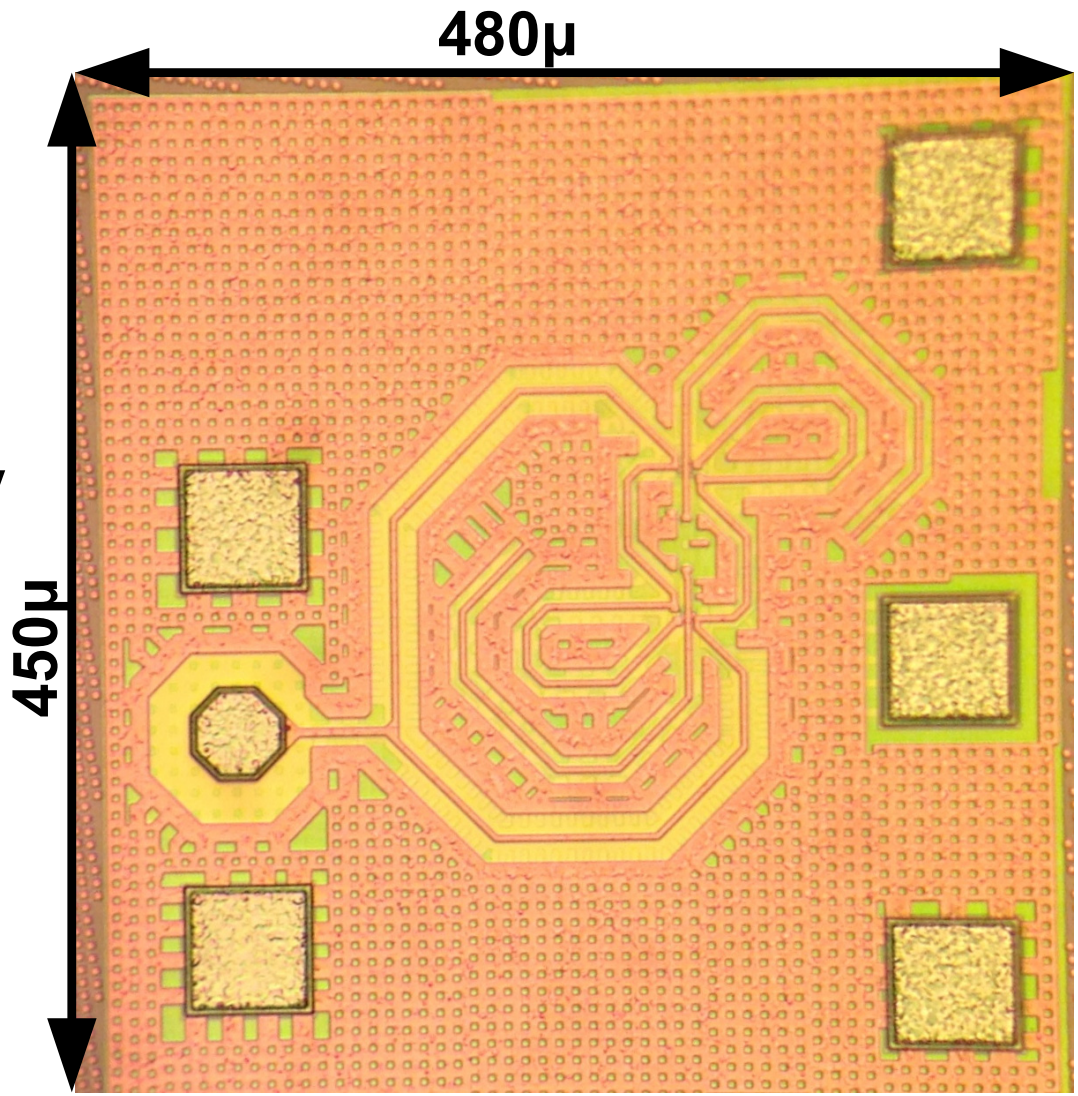
- Schematic of 2-stage VCO



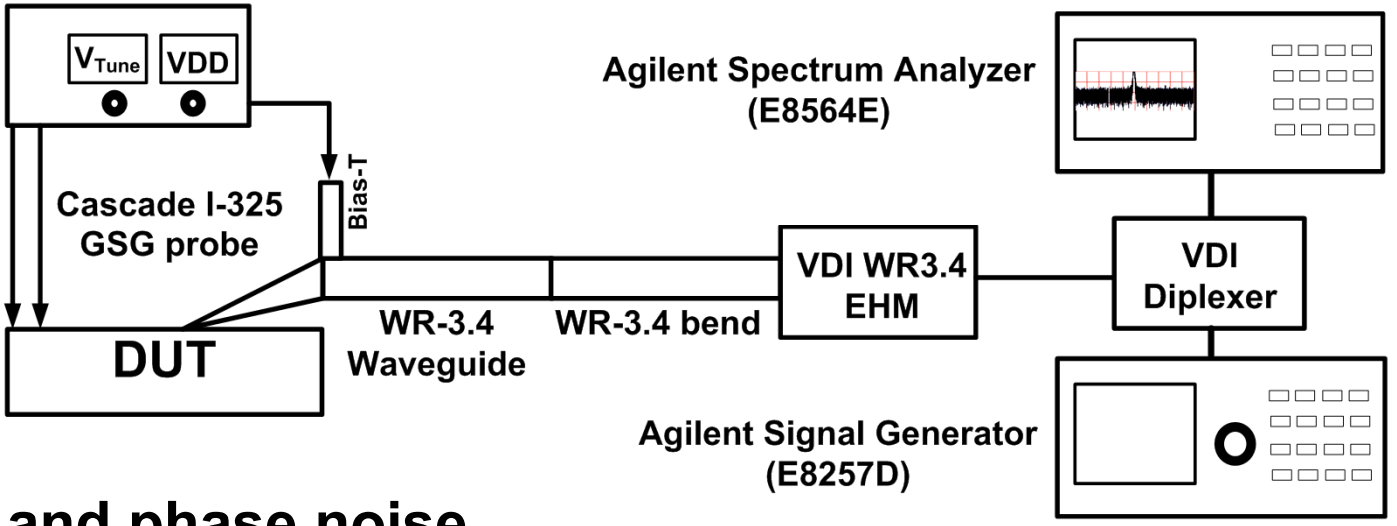


2-Stage VCO Prototype

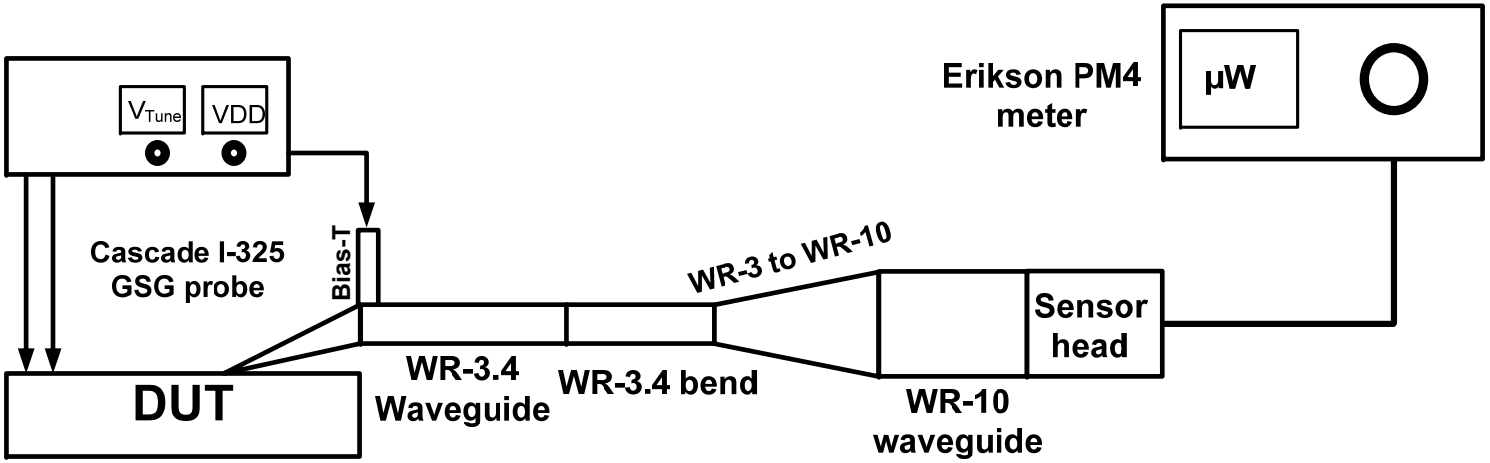
- Die photograph
- Implemented in a 65nm CMOS process
- The circuit consumes 37.8mW of power from 1.2V supply
- The output pad is designed to achieve 22fF capacitance required by output matching



Measurement Setup



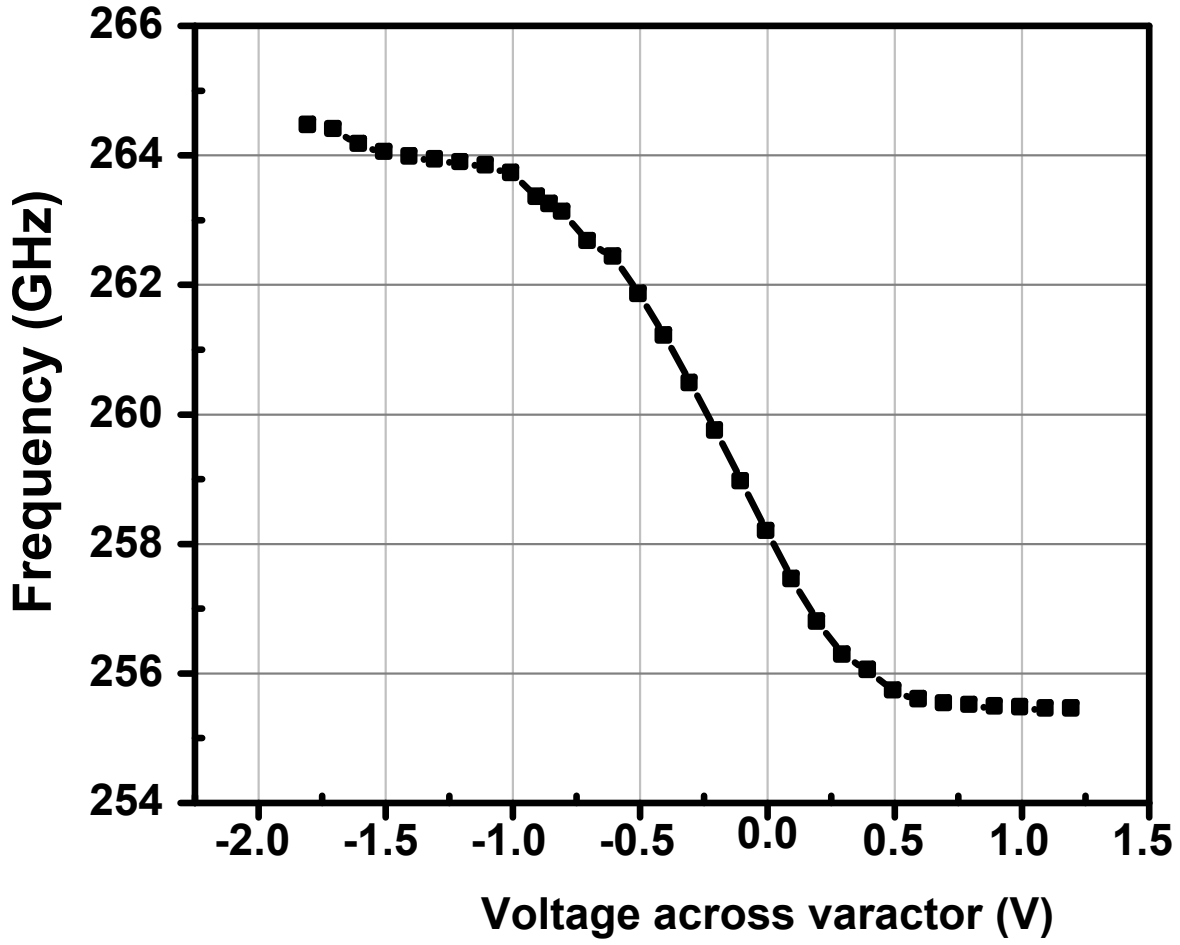
- **Frequency and phase noise**



- **Power measurement**

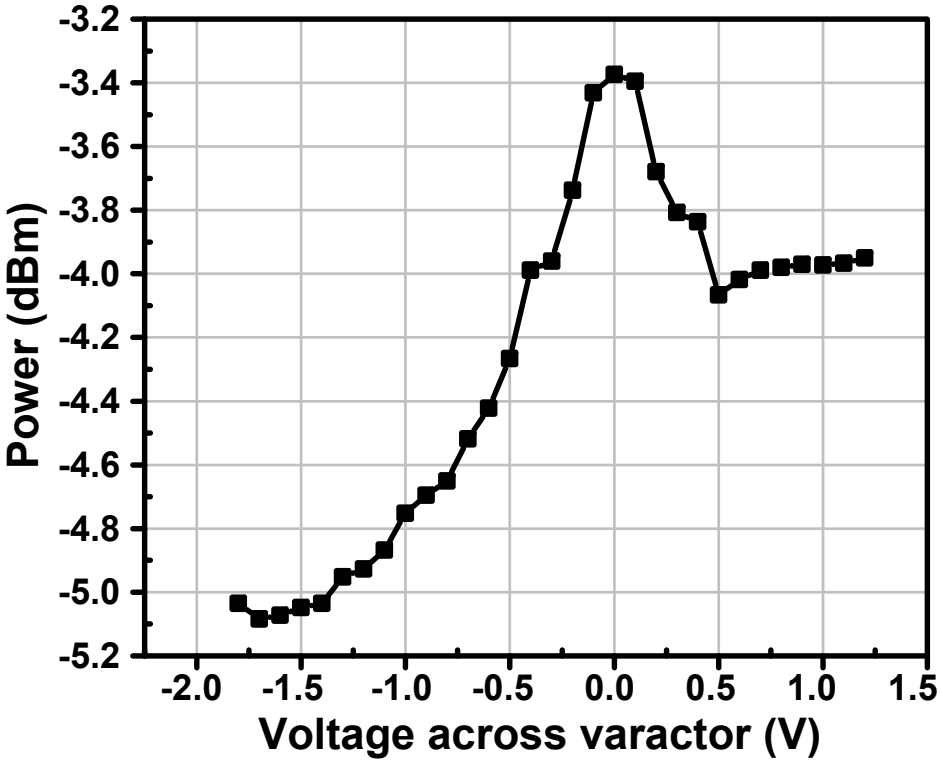
Frequency Measurement

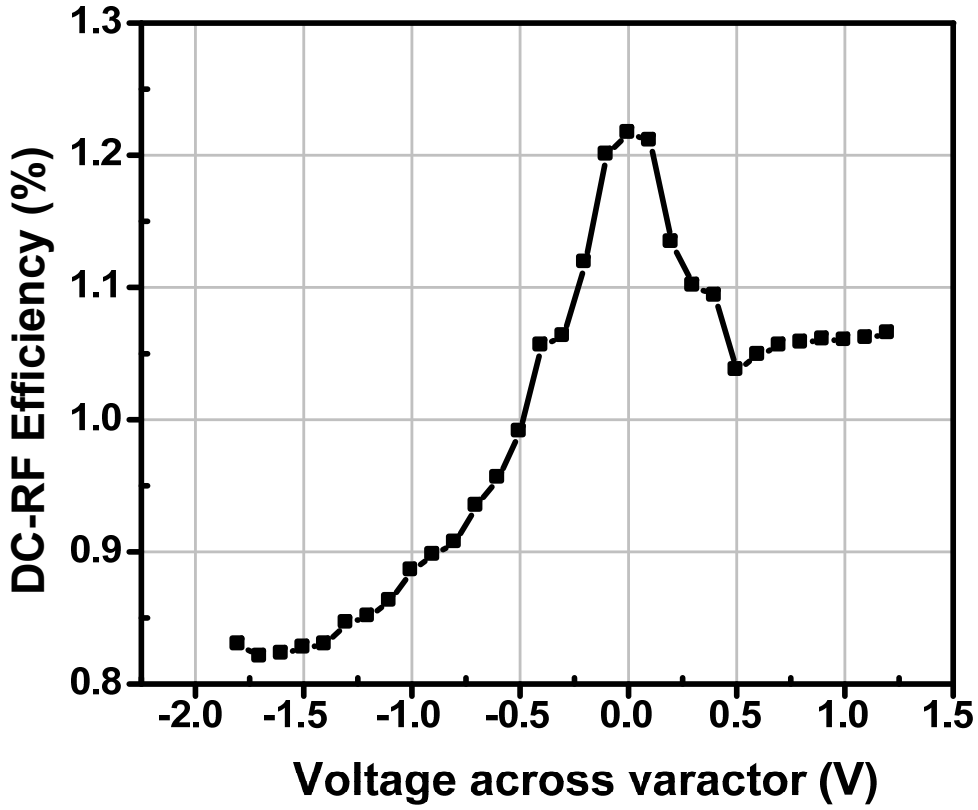
- Tuning range from 255GHz to 264.6GHz



Power Measurement

- The maximum power achieved is -3.4dBm
- The corresponding DC-RF efficiency is better than 1.2%
- DC-RF efficiency is always better than 0.8%





Comparison with Prior Art

Reference	ISSCC 2012	JSSC 2012	JSSC 2012	JSSC 2013	CSICS 2013	ISSCC 2012	ISSCC 2013	This work
Center Freq. (Ghz)	290	256	482	288	212	280	260	260
Peak output Power (dBm)	-1.2	-17	-7.9	-1.5	-7.1	-7.2	0.5	-3.4
DC-Power (mW)	325	71	61	275	30	810	800	37.8
Peak DC-to-RF (%)	0.23	0.03	0.27	0.3	0.65	0.023 (0.066)†	0.14 (0.33)†	1.2
Tuning range(%)	4.5	NA	NA	1.4††	2.8	3.2	1.4 (9.5)†††	3.7
Phase noise 1MHz offset (dBc/Hz)	-78	-88	-76	-87	NA	NA	-78	-79
Technology	65nm CMOS	130nm CMOS	65nm CMOS	65nm CMOS	130nm SiGe	45nm SOI CMOS	65nm CMOS	65nm CMOS
Output Measurement	Probing	Probing	Probing	Probing	Probing	Radiation	Radiation	Probing
Comments	No post processing	No post processing	No post processing	No post processing	No post processing	Wafer thinning	Hemispheric lens	No post processing

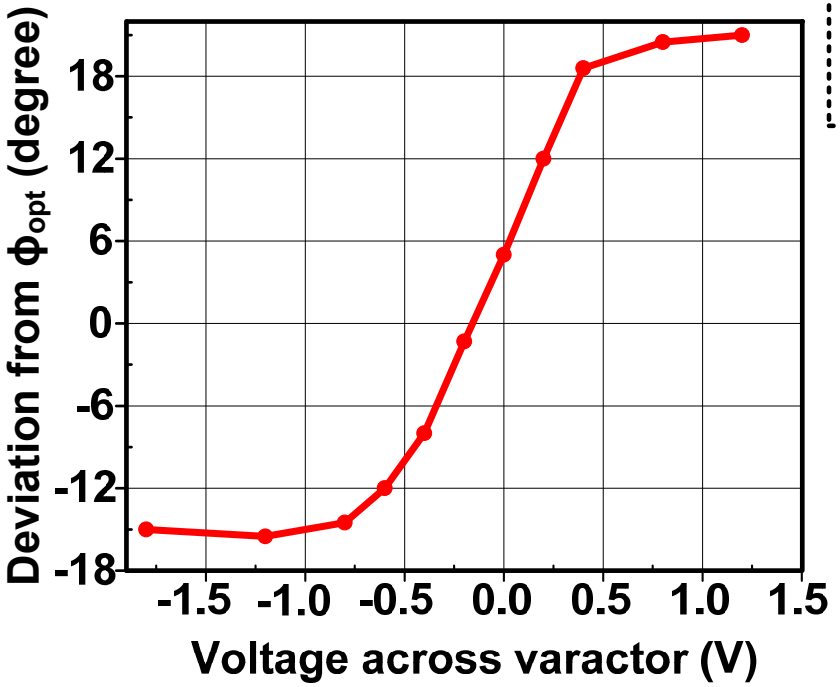
† Using power before antenna calculated with their respective radiation efficiencies.
†† Total tuning including changing supply voltage.
††† Not continuous tuning, performed via pulse modulation.

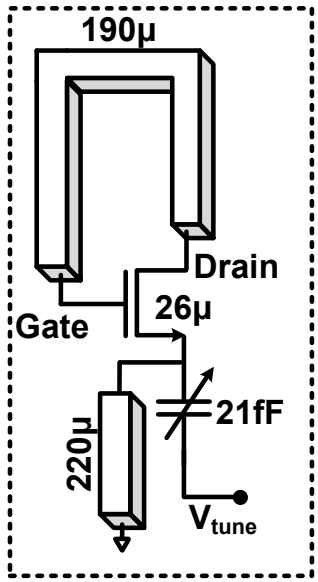
Outline

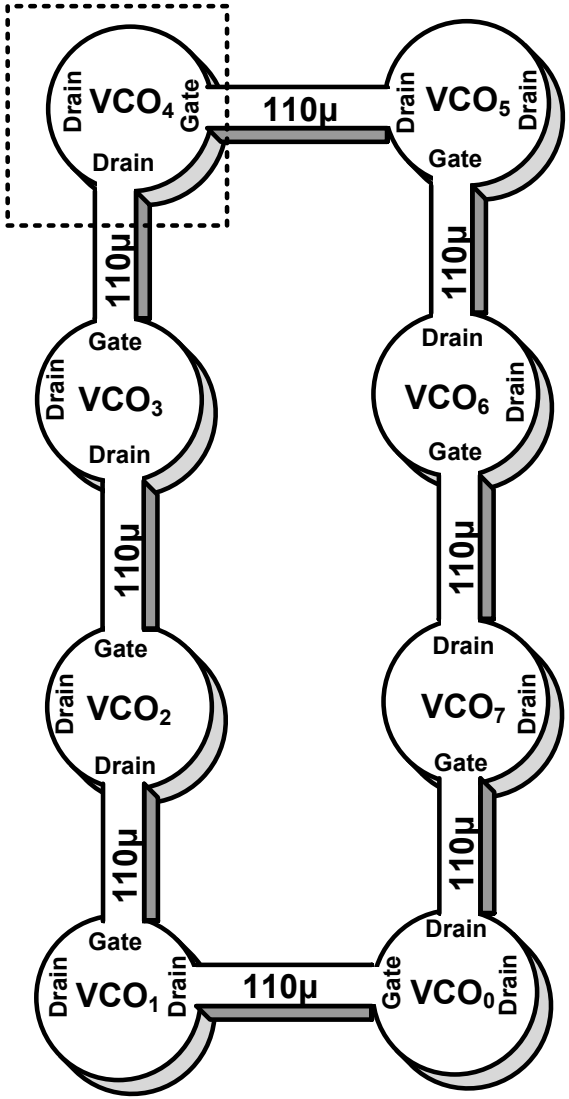
- Motivation
- A Scalable THz VCO Architecture
- A Source-degenerated Self-feeding VCO
- Passive Coupling & Harmonic Extraction
- Design of 2-stage VCO
- Design of 8-stage VCO
- Conclusion

8-Stage VCO Prototype

- Schematic of 8-stage VCO
- Optimal phase condition is satisfied

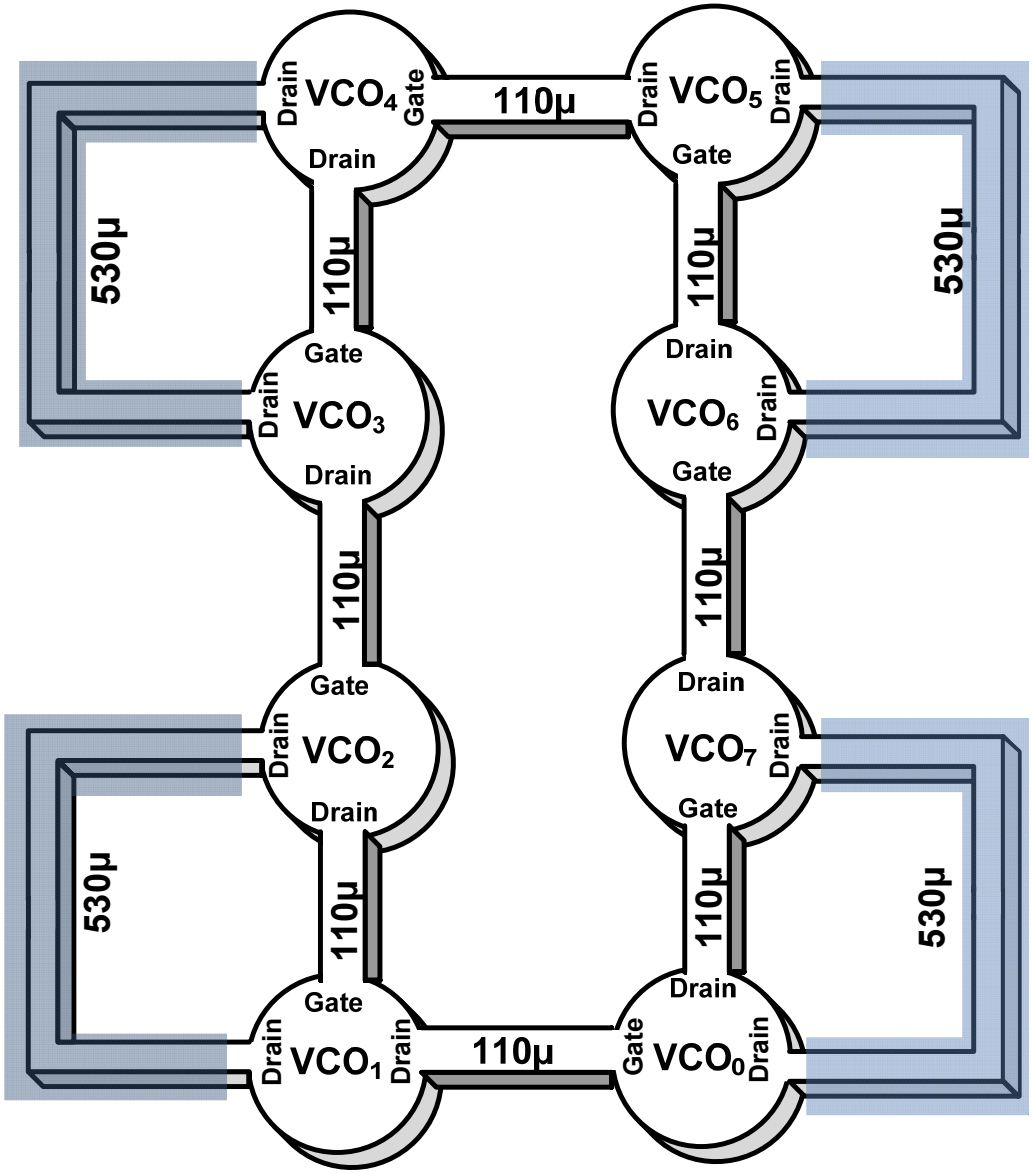






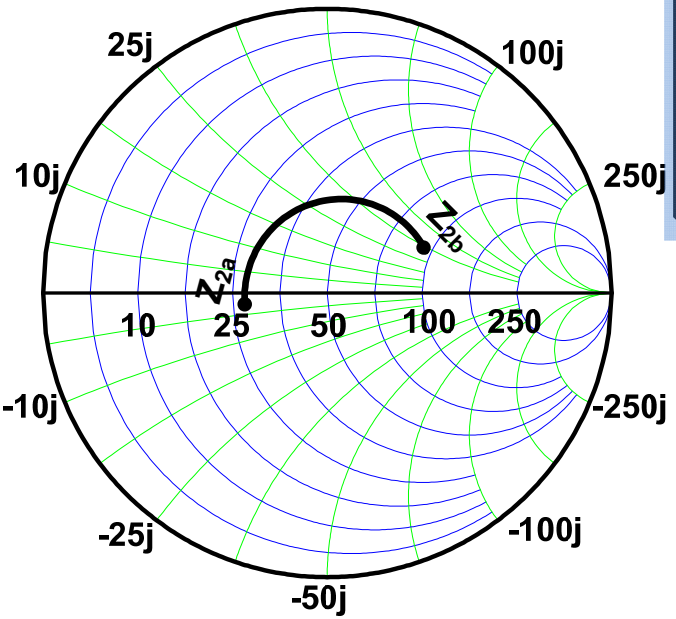
8-Stage VCO Prototype

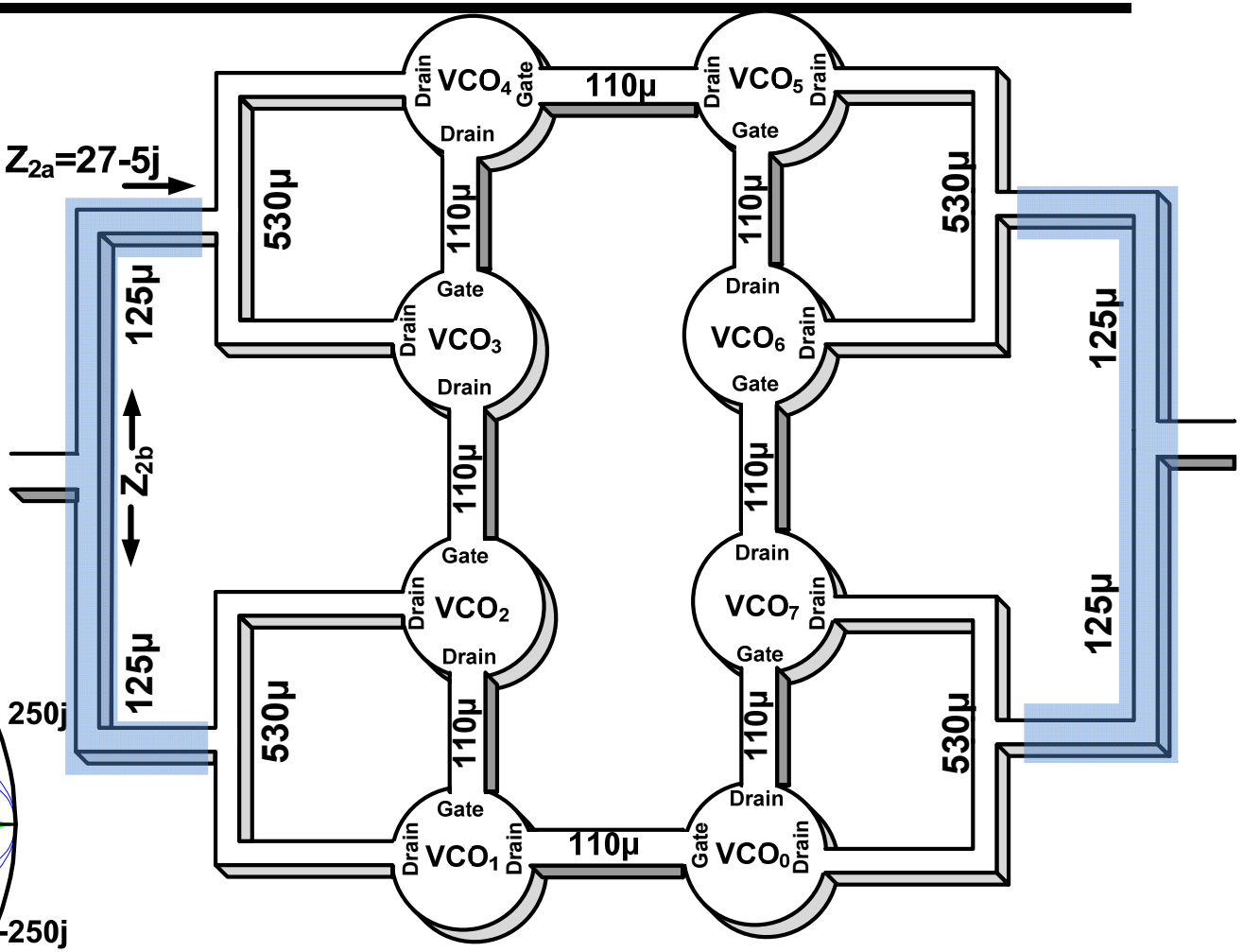
- **Harmonic extraction using 90 degree lines**



8-Stage VCO Prototype

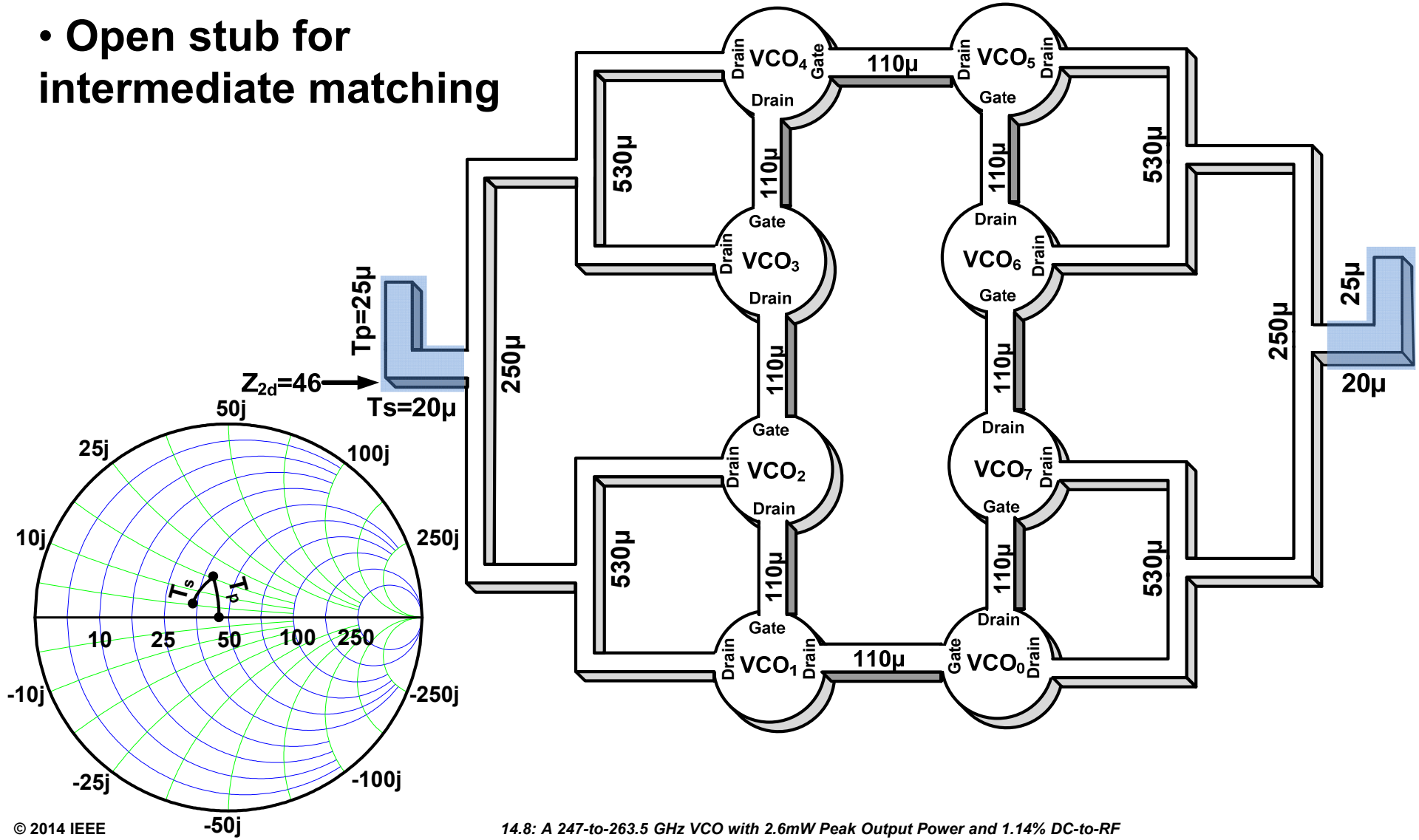
- Matching of 4-2 combiner





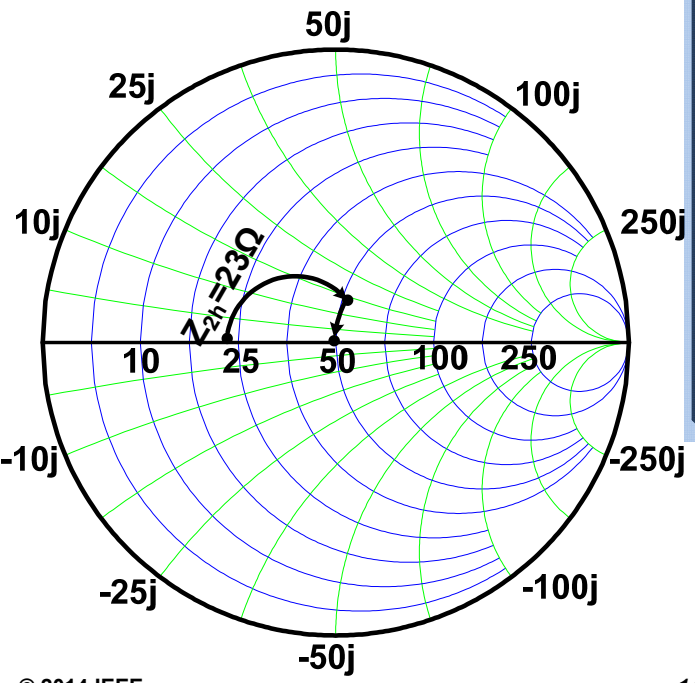
8-Stage VCO Prototype

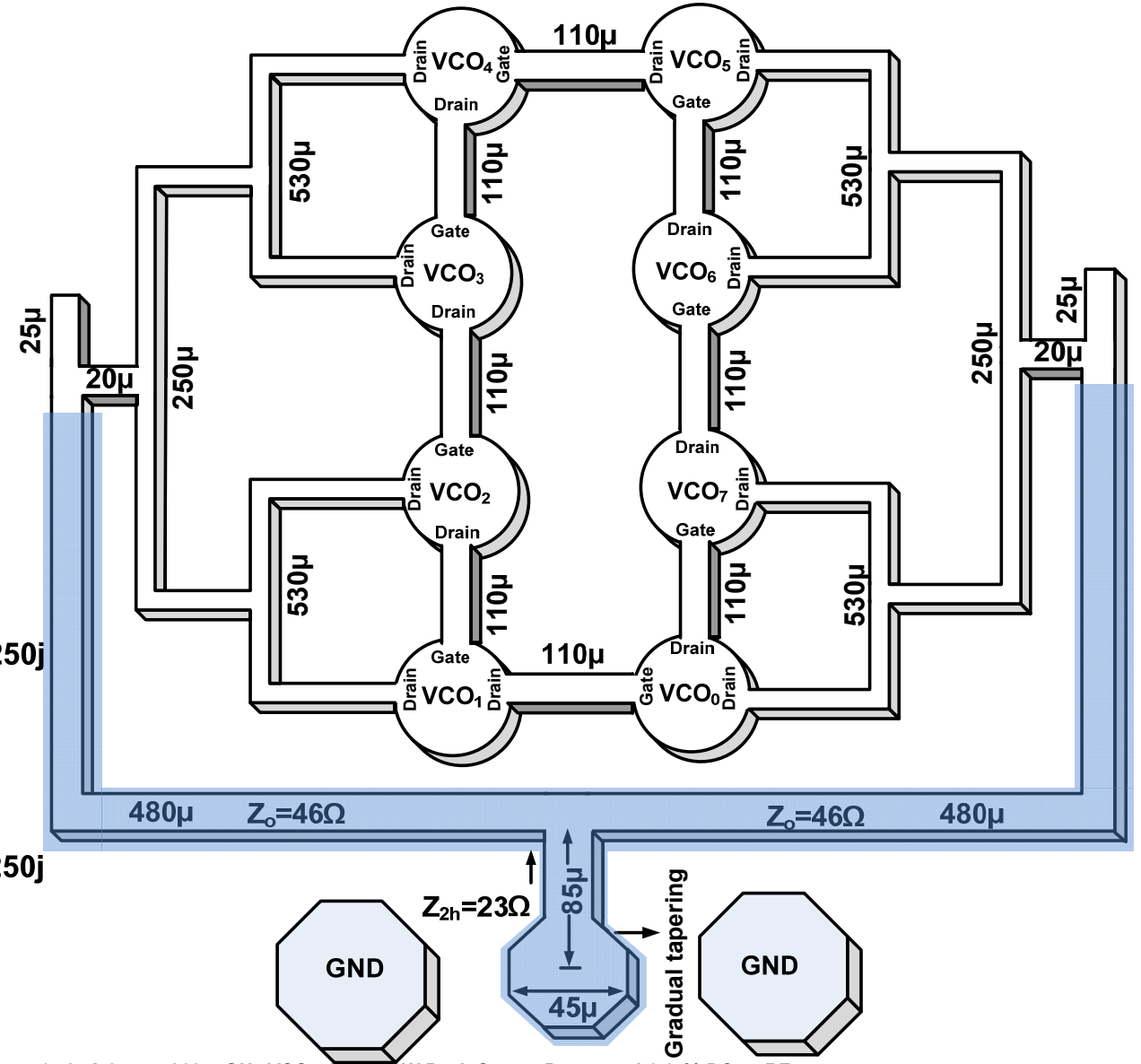
- **Open stub for intermediate matching**



8-Stage VCO Prototype

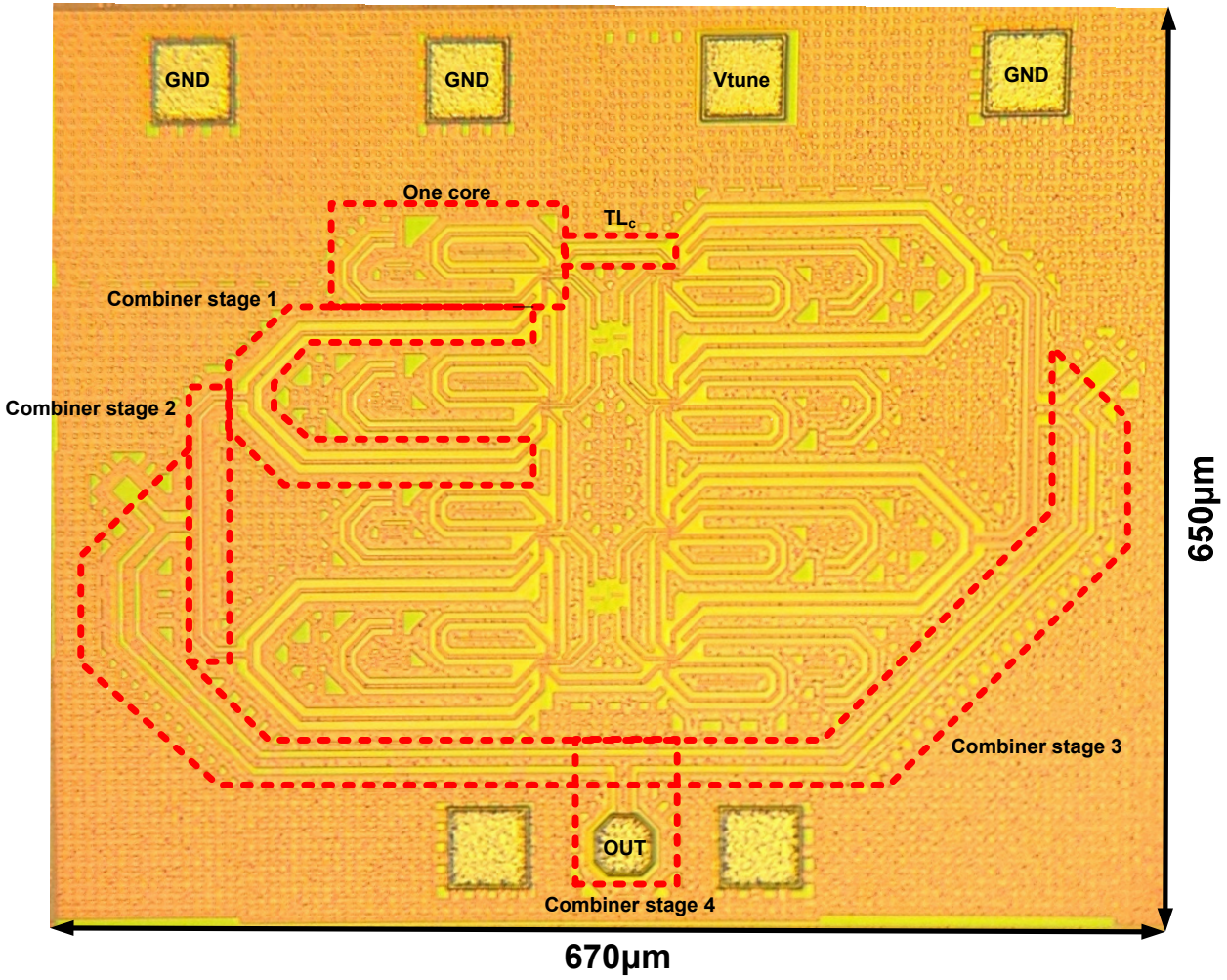
- Last stage output matching shown



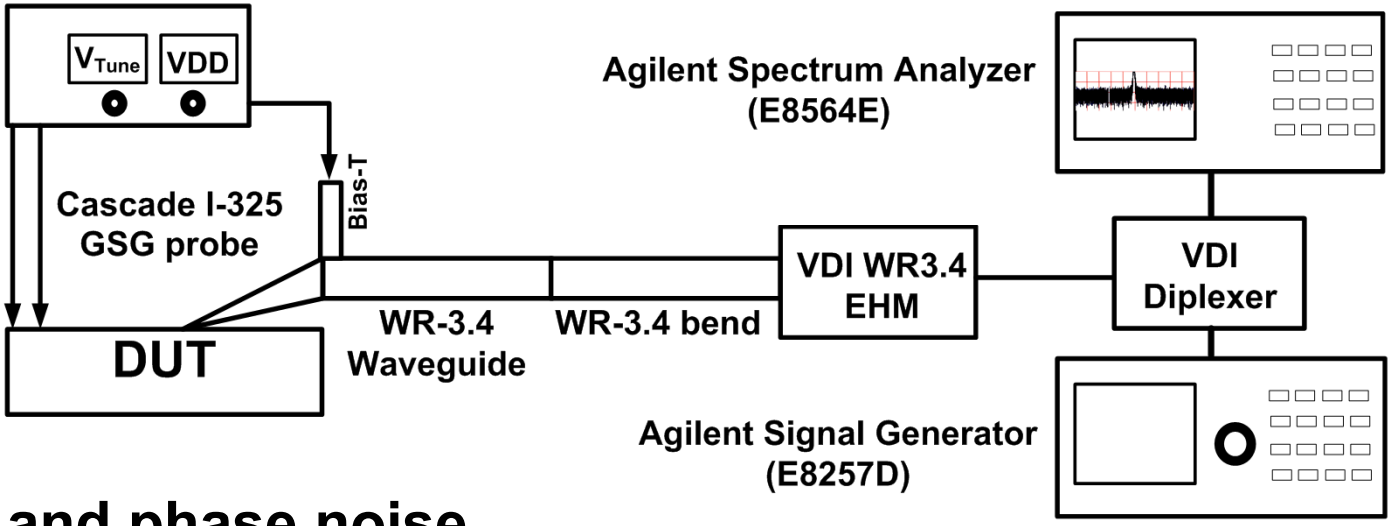


Chip Photograph

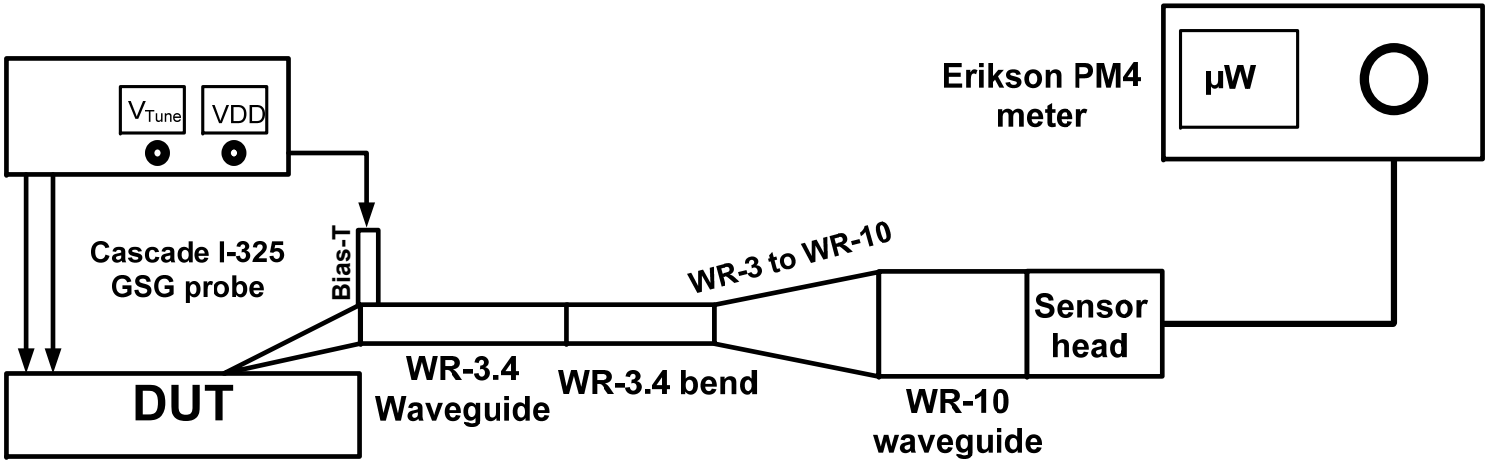
- Designed and implemented using 65nm bulk CMOS process



Measurement Setup



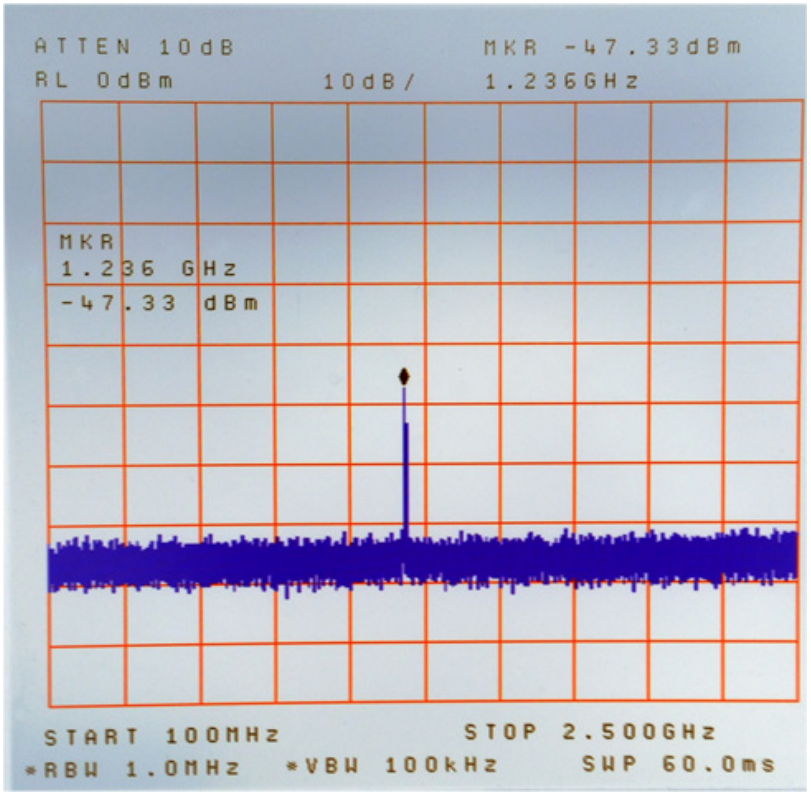
- **Frequency and phase noise**

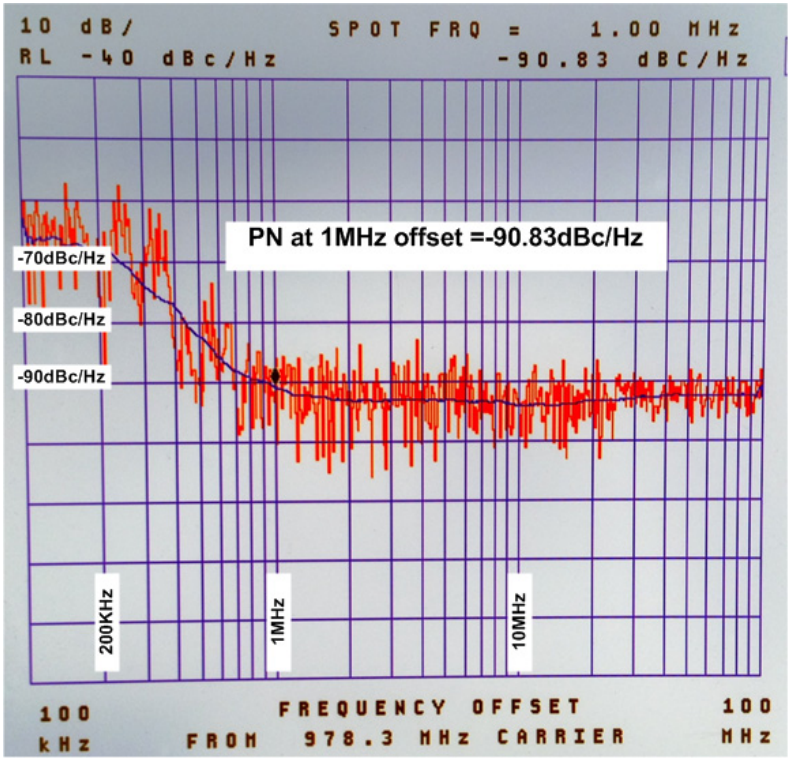


- **Power Measurement**

Spectrum and Phase noise

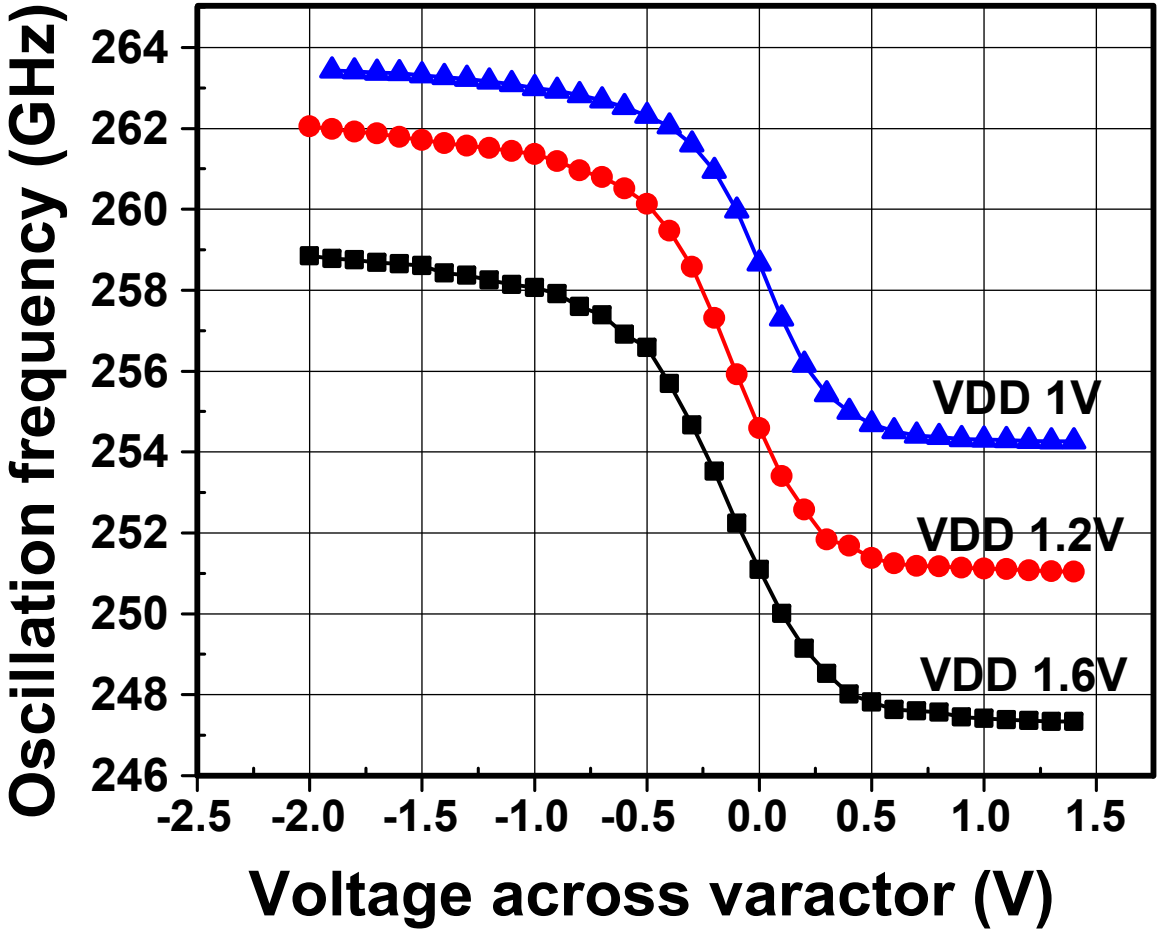
- Mix the RF signal with the 16th harmonic of the LO (~16 GHz)
- Frequency and phase noise is measured using down converted signal





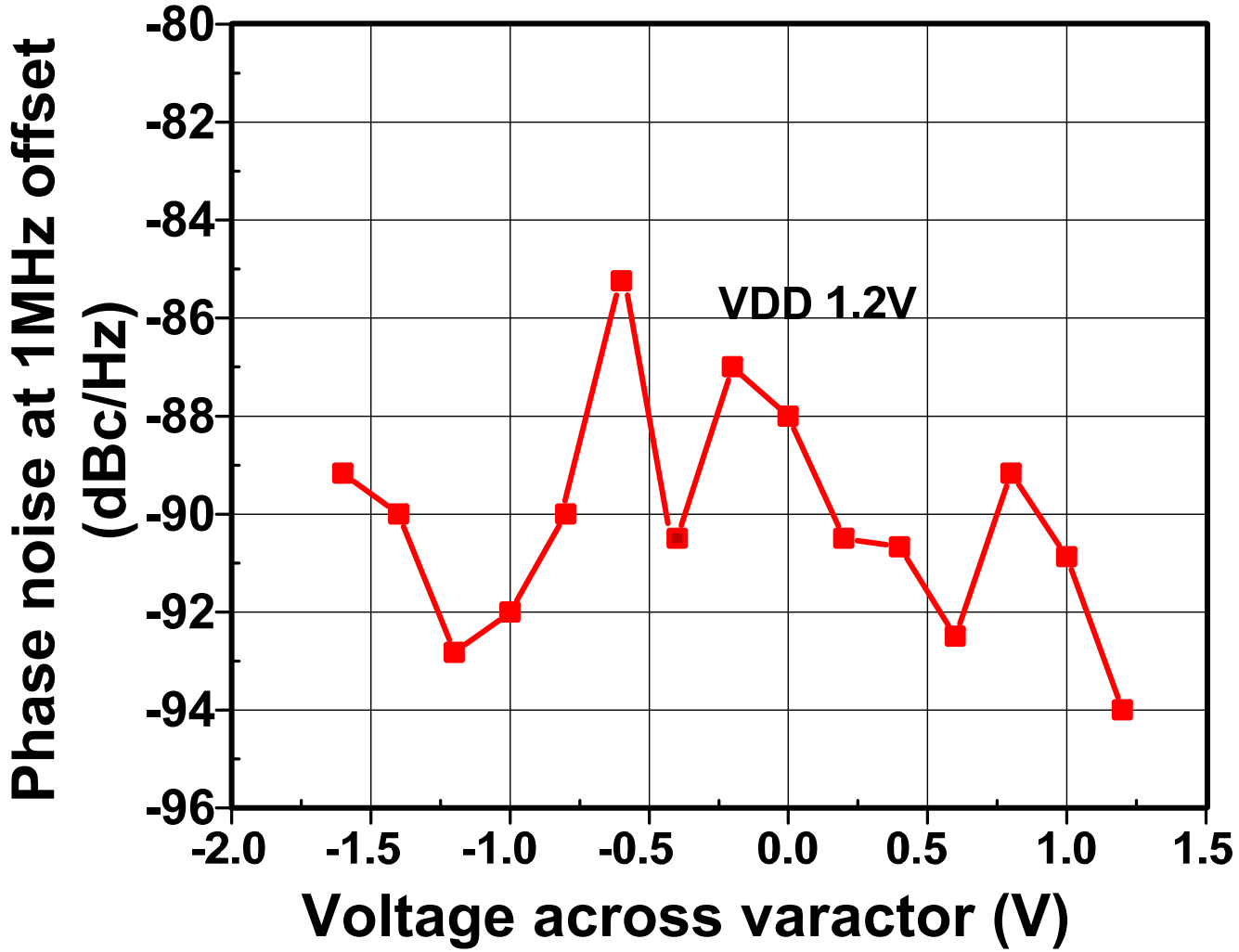
Frequency Measurement

- Frequency change at VDD of 1.2V is 12GHz.
- Frequency can be changed from 247-263GHz



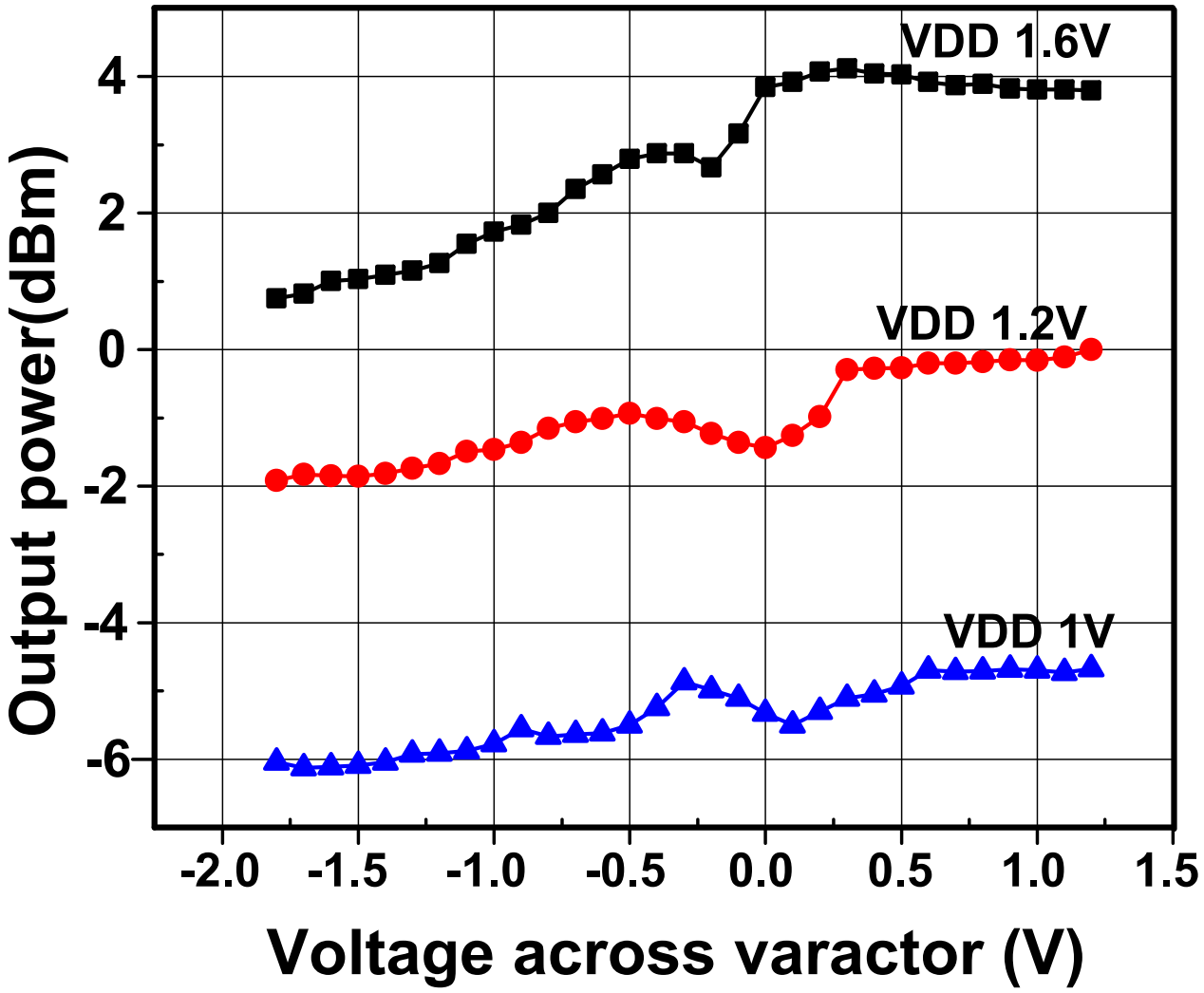
Phase Noise Measurement

- Phase noise vary from -85dBc/Hz to -94dBc/Hz.



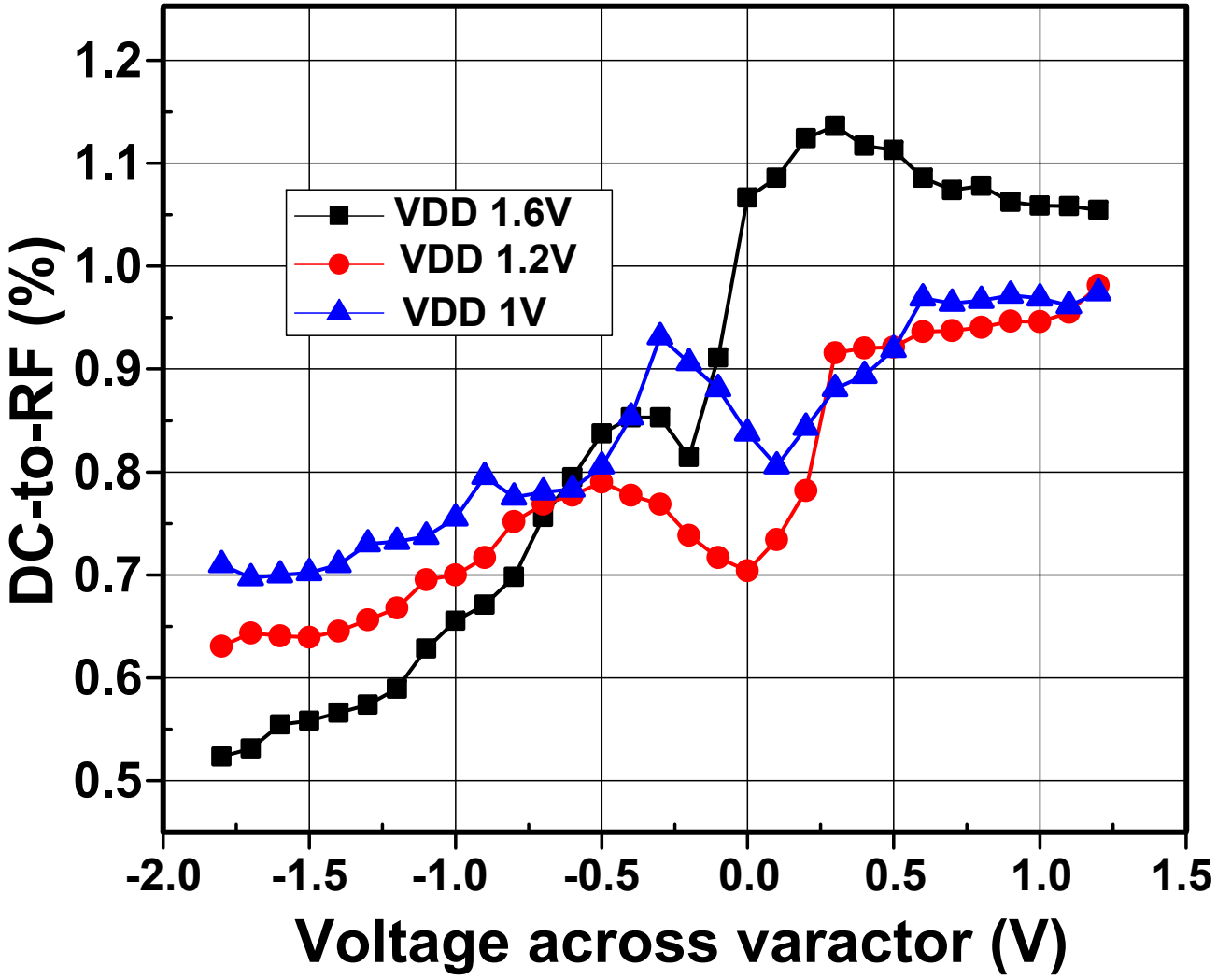
Output Power

- The maximum measured power is 4.1dBm.



Efficiency Measurement

- Maximum DC-RF efficiency is 1.15%



Outline

- Motivation
- A Scalable THz VCO Architecture
- A Source-degenerated Self-feeding VCO
- Passive Coupling & Harmonic Extraction
- Design of 2-stage VCO
- Design of 8-stage VCO
- Conclusion

Comparison with Prior Art

Reference	ISSCC 2012	JSSC 2012	JSSC 2012	JSSC 2013	CSICS 2013	ISSCC 2012	ISSCC 2013	This work
Center Freq. (Ghz)	290	256	482	288	212	280	260	256
Peak output Power (dBm)	-1.2	-17	-7.9	-1.5	-7.1	-7.2	0.5	4.1
DC-Power (mW)	325	71	61	275	30	810	800	227
Peak DC-to-RF (%)	0.23	0.03	0.27	0.3	0.65	0.023 (0.066)†	0.14 (0.33)†	1.14
Tuning range(%)	4.5	NA	NA	1.4 ††	2.8	3.2	1.4 (9.5)†††	4.3 (6.5)††
Phase noise 1MHz offset (dBc/Hz)	-78	-88	-76	-87	NA	NA	-78	-94
Technology	65nm CMOS	130nm CMOS	65nm CMOS	65nm CMOS	130nm SiGe	45nm SOI CMOS	65nm CMOS	65nm CMOS
Output Measurement	Probing	Probing	Probing	Probing	Probing	Radiation	Radiation	Probing
Comments	No post processing	No post processing	No post processing	No post processing	No post processing	Wafer thinning	Hemispheric lens	No post processing

† Using power before antenna calculated with their respective radiation efficiencies.

†† Total tuning including changing supply voltage.

††† Not continuous tuning, performed via pulse modulation.

Conclusions

- Proposed a scalable architecture to achieve high power, efficiency and tunability.
- Source-degenerated self feeding VCO is employed for highest power and passive coupling.
- Harmonic extraction efficiency is improved.
- Proposed methodology is employed to design 2-stage and 8-stage VCOs.
- Experimental results of a fabricated CMOS source in 65nm process proves feasibility of this approach.

Acknowledgments

- TSMC University Shuttle Program for chip fabrication
- NSF, ARL, and ONR for support
- Dr. Paul Maki and Dr. Alfred Hung
- EM simulation support from Sonnet
- Dr. R. Han, Dr. Y. Tousi, Prof. O. Momeni and all the members of UNIC lab from Cornell University